OB2201

High Performance Quasi-Resonant PWM Controller

Product Specification

GENERAL DESCRIPTION

OB2201 is a high performance flyback Quasi-Resonant (QR) controller optimized to achieve high efficiency in the universal input range and full loading range with effective system cost.

At full loading, the IC operates in fix frequency (52KHz) CCM mode in the low line input range and operates in QR mode in high line input range. In this way, high efficiency in the universal input range at full loading can be achieved.

At normal load condition, it operates in QR mode. To minimize switching loss, the maximum switching frequency in QR mode is internally limited to 90 KHz. When the loading goes low, it operates in PFM mode for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

OB2201 offers comprehensive protection coverage including Cycle-by-Cycle Current Limiting (OCP), VCC Under Voltage Lockout (UVLO), Output Over Voltage Protection (OVP), Over Temperature Protection (OTP), Over Load Protection (OLP), VCC Over Voltage Protection (VCC OVP), VCC Clamp, and Gate Clamp. OB2201 also features protections against pin open and short conditions on selected pins.

OB2201 is offered in SOP-8 and DIP-8 packages.

FEATURES

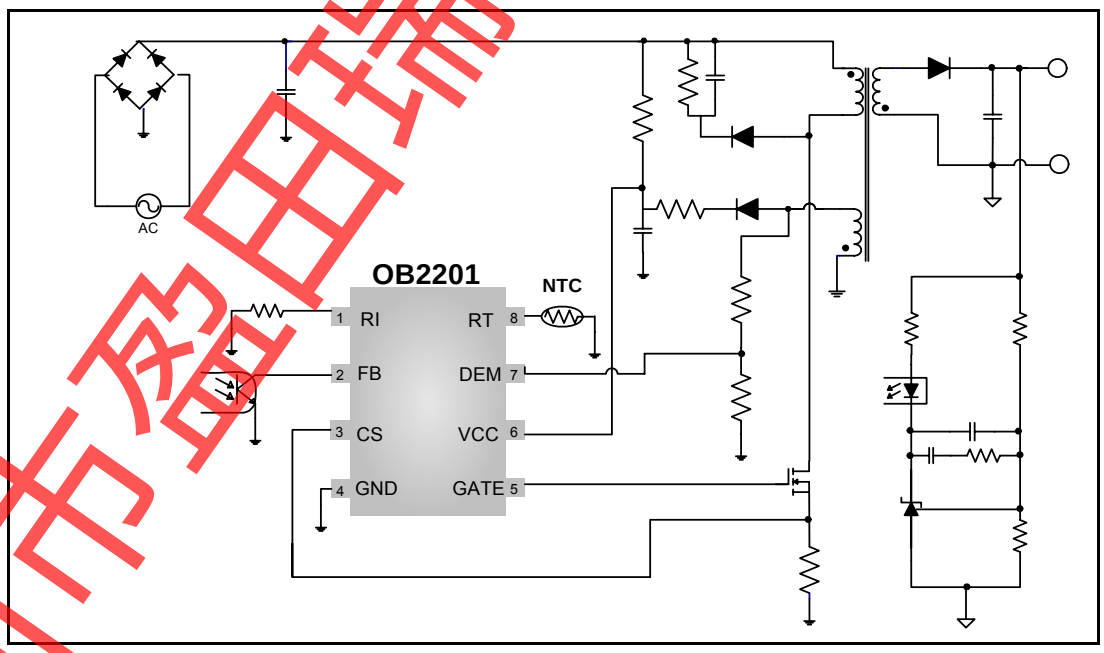
- Multi-Mode Operation:
  - At Full Loading, Fix Frequency (52KHz) CCM Operation @ Low Line and QR Mode Operation @ High Line Input
  - Quasi-Resonant Operation at Normal Load
  - Pulse Frequency Modulation (PFM) Operation at Light Load
  - Burst Mode at No Load
- Adaptive Frequency Shuffling and Slope Compensation @ Fix Frequency CCM Mode
- Programmable OTP with latch Shutdown
- Fixed 4ms Soft-start
- 2.5us Minimum Off Time
- 12.5us Maximum On Time Limit
- 55us Maximum Off Time Limit
- 90KHz Maximum Frequency Limit
- Internal Leading Edge Blanking
- Output Over Voltage Protection
- 800mA Peak Current Sink/Source Capability

APPLICATIONS

Offline AC/DC flyback converter for

- Power Adaptor and Open-frame SMPS
- Set-Top Box Power Supplies
- NB/DVD

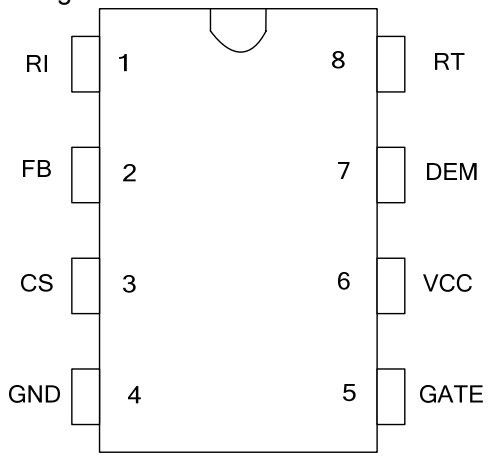
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of OB2201 in DIP8 and SOP8 package is shown as below.



Ordering Information

Part Number	Description
OB2201AP	8 Pin DIP, Pb free in Tube
OB2201CP	8 Pin SOP, Pb free in Tube
OB2201CPA	8 Pin SOP, Pb free in T&R

Note: All Devices are offered in Pb-free Package if not otherwise noted.

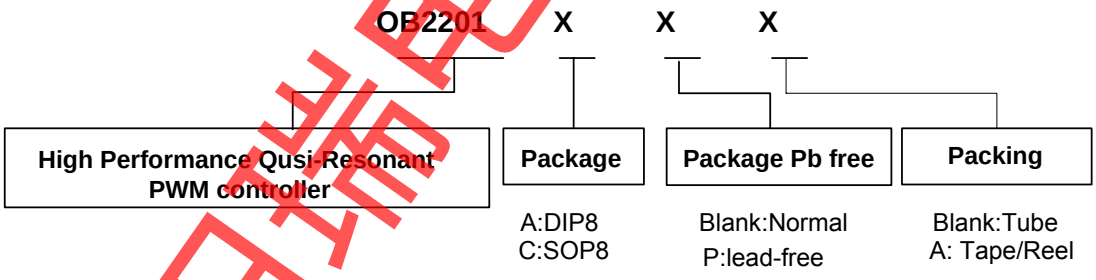
Package Dissipation Rating

Package	RθJA (℃/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

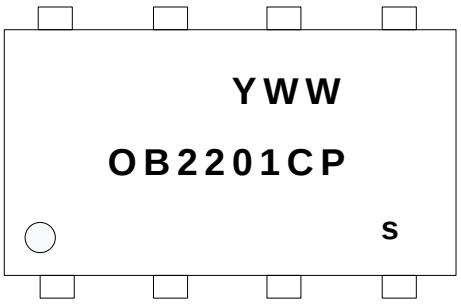
Parameter	Value
VCC Zener Clamp Voltage	29 V
VCC Clamp Continuous Current	10 mA
RI Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
DEM Input Voltage	-0.7 to 7V
RT Input Voltage	-0.3 to 7V
Maximum Operating Junction Temperature T_J	150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

SOP8



Y: Year Code (0-9)

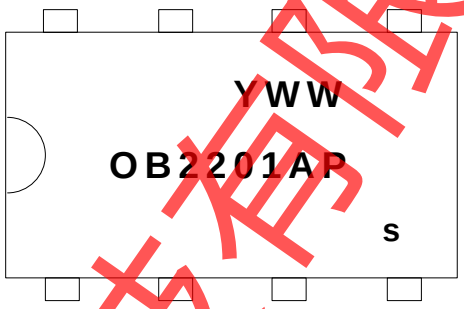
WW: Week Code (1-52)

C: SOP8

P:lead-free

s: internal code

DIP8



Y: Year Code (0-9)

WW: Week Code (1-52)

A: DIP8

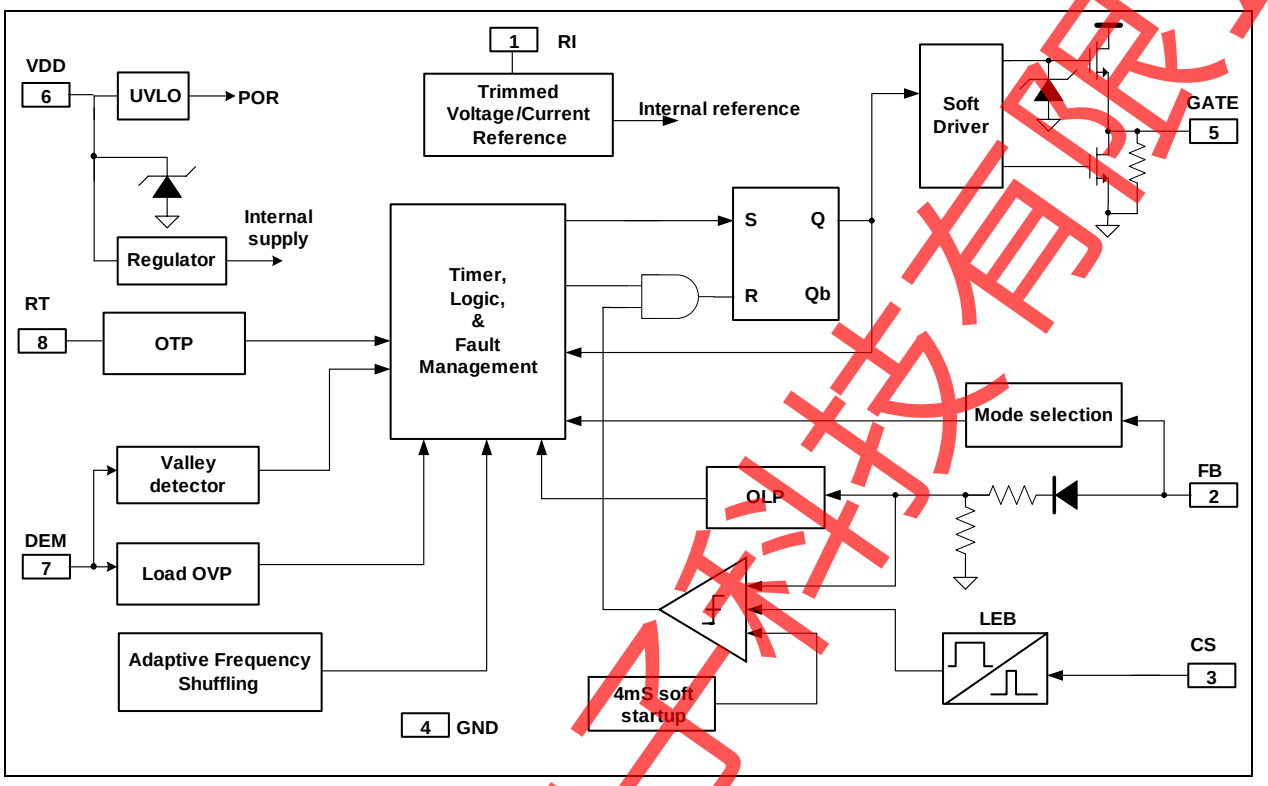
P:lead-free

s: internal code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	RI	I	A resistor connected between RI and GND sets the internal frequency and timer. The resistor is recommended to be set in the vicinity of 20K Ohm.
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 3.
3	CS	I	Current sense input.
4	GND	P	Ground for internal circuitry.
5	GATE	O	Totem-pole gate drive output for power MOSFET.
6	VCC	P	Chip DC power supply pin.
7	DEM	I	Transformer core demagnetization detection pin. This pin is also used for output over voltage protection (OVP).
8	RT	I	Over Temperature Protection pin. Connected through a NTC resistor to GND for over temperature latch shutdown.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VCC	VCC Supply Voltage	12	28	V
T_A	Operating Ambient Temperature	-20	85	°C

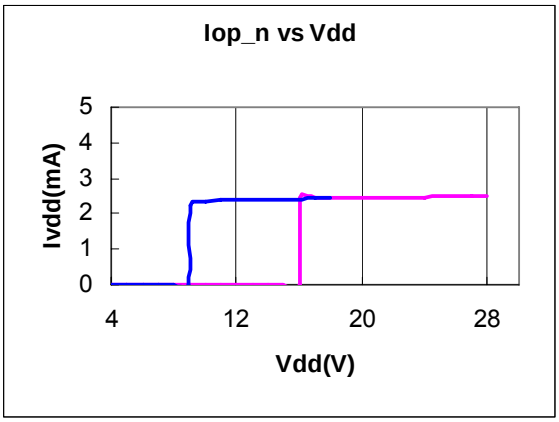
ELECTRICAL CHARACTERISTICS

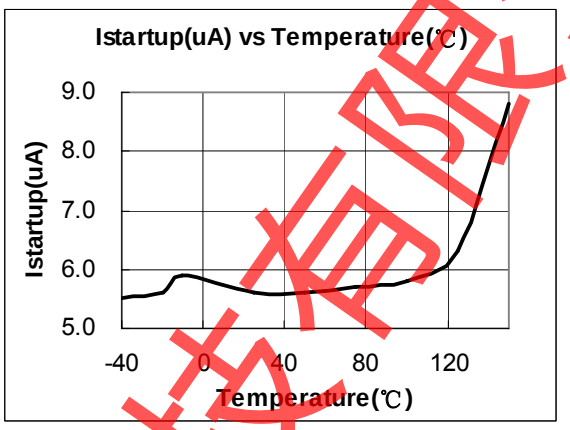
(T_A = 25°C, VCC=16V, RI=20K Ohm if not otherwise noted)

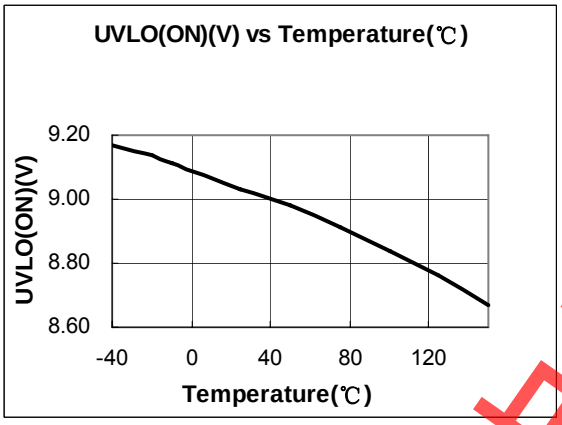
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VCC Pin)						
I_VCC_Startup	VCC Start up Current	VCC =UVLO(OFF)-1.5V, Measure current into VCC	-	5	15	uA
I_VCC_quiet	Operation Current without switching	FB=3V	-	2.0	4.0	mA
I_VCC_operation	Operation current with switching	FB=3V, 1nF load at GATE	-	3.0	5.0	mA
UVLO(ON)	VCC Under Voltage Lockout Enter		8.0	9.0	10.0	V
UVLO(OFF)	VCC Under Voltage Lockout Exit (Startup)		15	16	17	V
OVP(ON)	VCC Over Voltage Protection Enter			28		V
VCC_Clamp	VCC Zener Clamp Voltage	I_VCC = 5 mA		29		V
Feedback Input Section (FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$	-	3.5	-	V/V
V_{FB}_Open	FB Open Voltage		--	5.3	--	V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND, measure current	--	1.5	-	mA
V_{TH}_BM_on	Burst Mode on threshold		-	0.8	-	V
V_{TH}_BM_off	Burst Mode off threshold		-	0.7	-	V
V_{TH}_PL	Power Limiting FB Threshold Voltage		-	4.4	-	V
T_D_PL	Power limiting Debounce Time		--	80	--	ms
Z_{FB}_IN	Input Impedance		-	4	-	Kohm
Current Sense Input Section (CS Pin)						
T_blanking	CS Input Leading Edge Blanking Time		-	300	-	ns
V_{TH}_OCP_zero_ontime	Internal current limiting threshold	Zero duty cycle	0.415	0.45	0.485	V
V_{TH}_OCP_max	Internal current limiting threshold	Maximum duty cycle	-	0.80	-	V
V_{TH}_CS_min	Flodback mode and burst mode CS peak			0.3		V
T_D_OC	Over Current Detection and Control Delay	CL=1nf at GATE,	-	100	--	ns
Demagnetization Detection Section (DEM Pin)						
V_{TH}_DEM	Demagnetization comparator threshold voltage		--	75	--	mV
V_{DEM}_clamp(neg)	Negative clamp voltage		-	-0.7	-	V
V_{DEM}_clamp(pos)	Positive clamp voltage		-	6.0	-	V
T_{supp}	Suppression of the transformer ringing at start of secondary stroke		--	2.5	--	us
T_{OUT}	Timeout after last demag transistion		--	5	--	us
T_{DEM_delay}	Demag propagation delay		-	250	-	ns

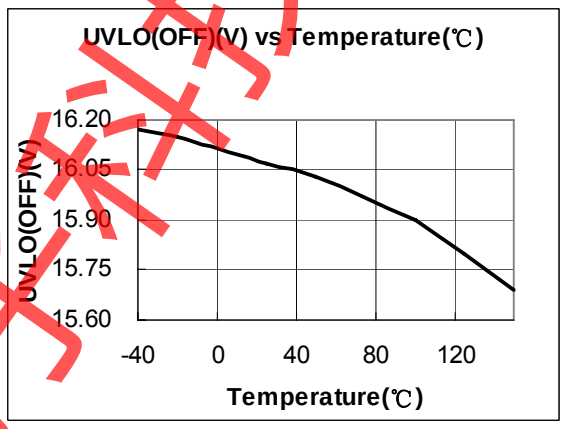
V_{TH}_OVP	Output OVP trigger point		-	3.75	-	V
T_OVP_delay	Number of subsequent cycles to be true OVP		-	4	-	Cycle
Soft Start Section						
T_soft	Internal soft startup			4		ms
Timer Section						
RI_range	Operating RI resistor range		14	20	26	Kohm
V_RI_open	RI open voltage			2.0		V
Fburst	Burst mode switching frequency	RI=20K	-	22	-	KHz
Fmax_QR_H	Frequency high clamp in QR mode	RI=20K	82	90	98	KHz
Fmin_QR_L	Frequency low clamp in QR mode	RI=20K	47	52	57	KHz
△F（shuffle）/F	Fmin_QR_L frequency shuffling range		-4		+4	%
Ton_max	Maximum on time	RI=20K	10	12.5	15	us
Toff_max	Maximum off time	RI=20K	40	55	75	us
G_PFM	PFM mode frequency modulation slope versus control voltage		-	90	-	KHz/V
Over temperature Protection						
I_RT	Output current of RT pin,	RI=20K		100		uA
Vth_OTP	OTP threshold voltage		1.00	1.05	1.10	V
V_RT_open	RT pin open voltage			3.5		V
Latch Protection						
V_latch_release	VCC latch release voltage		--	6.3	--	V
Ivdd(latch)	VCC current when latch off	VCC=V_latch_release+1V	-	45	-	uA
Gate Drive Output (GATE Pin)						
VOL	Output Low Level	Io = 100 mA (sink)	-	-	1	V
VOH	Output High Level	Io = 100 mA (source)	7.5	-	-	V
VG_Clamp	Output Clamp Voltage Level	VCC=20V	-	16.5	-	V
T_r	Output Rising Time	CL = 1nf	-	80	-	ns
T_f	Output Falling Time	CL = 1nf	-	30	-	ns

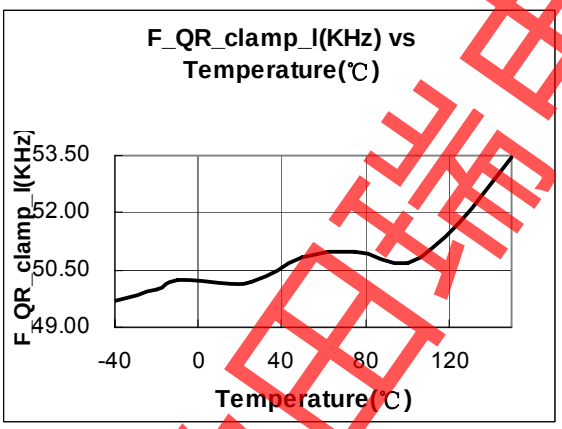
CHARACTERIZATION PLOTS

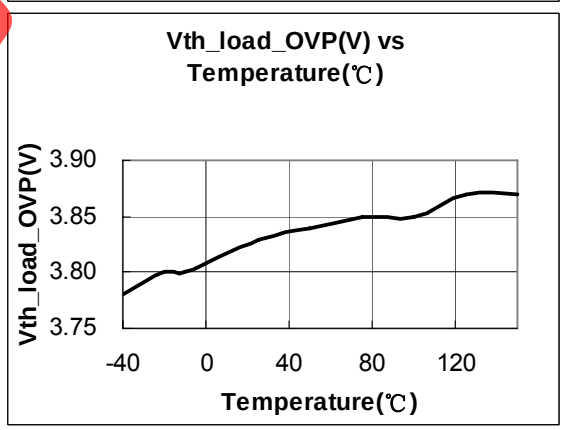


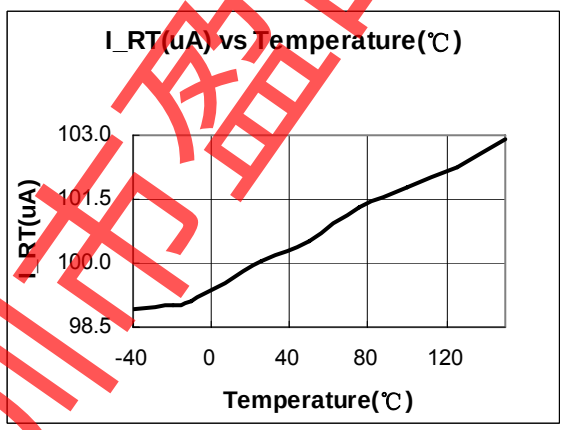


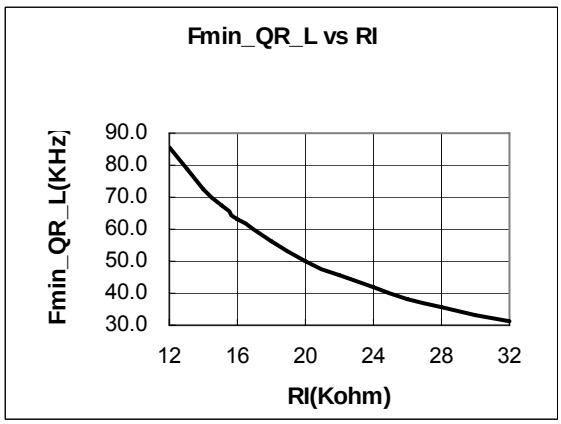












OPERATION DESCRIPTION

Quasi-Resonant (QR) converter typically features lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency. OB2201 is a highly integrated QR controller optimized for offline flyback converter applications. The built-in advanced energy saving with high level protection features provide cost effective solutions for energy efficient power supplies.

- **Startup Current and Start up Control**

Startup current of OB2201 is designed to be very low so that VCC could be charged up above UVLO(OFF) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2MΩ, 1/8 W startup resistor could be used together with a VCC capacitor to provide a fast startup and yet low power dissipation design solution.

- **Operating Current**

The operating current of OB2201 is as low as 3mA. Good efficiency is achieved by the low operating current together with extended burst mode control schemes at No/light load conditions.

- **Multi-Mode Operation for High Efficiency**

OB2201 is a multi-mode QR controller. The controller changes the mode of operation according to FB voltage, which reflects the line and load conditions.

■ At full load conditions (FB>Vth3, Figure 1), there are two situations: firstly, if the system input is in low line input range, the IC operates in fix frequency (52KHz @ RI=20K Ohm) CCM mode. Thus, small size transformer can be used with high power conversion efficiency. Secondly, if the system input is in high line input range, the IC operates in QR mode. In this way, high power conversion efficiency can be achieved in the universal input range when system is at full loading conditions.

■ At normal operating conditions (Vth2<VFB<Vth3, Figure 1), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when 90KHz frequency clamping is reached.

■ At light load conditions (Vth1<VFB<Vth2, Figure 1), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. In PFM mode, the "ON" time in a switching cycle is fixed and the system modulates the frequency according to the load conditions. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency foldback is realized and high power conversion efficiency is achieved.

■ At zero load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In this condition, voltage at FB is below burst mode threshold level, Vth1. The Gate drive output switches only when VCC voltage drops below a preset level or FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. In extended burst mode, the switching frequency is fixed to 22KHz, in this way, possible audio noise is eliminated.

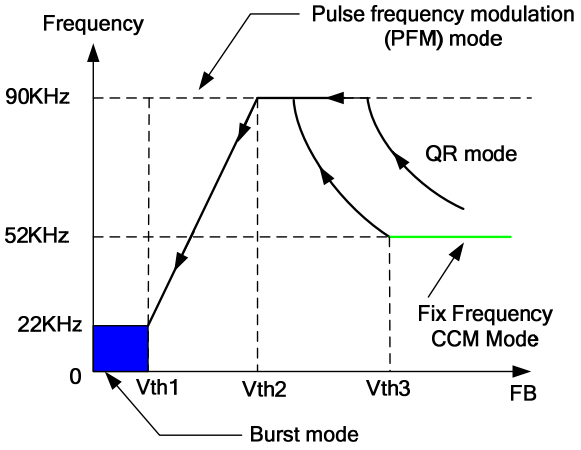


Figure 1

- **Internal frequency and timer setting**

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the internal frequency and timer is determined. It is recommended that the resistor is set to be in the vicinity of 20K Ohm.

- **Demagnetization Detection**

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. This voltage features a flyback polarity. A new cycle starts when the power switch is activated. After the on time (determined by the CS voltage and FB), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

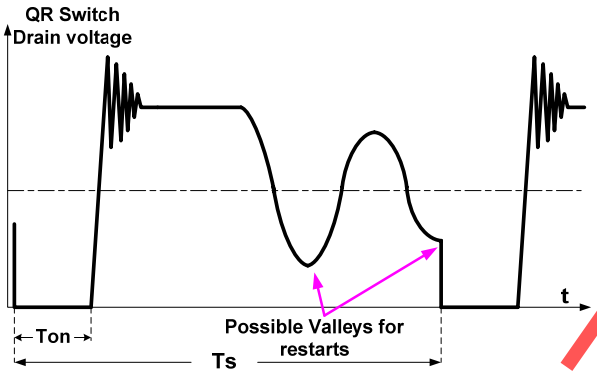


Figure 2

The typical detection level is fixed at 75mV at the DEM pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at DEM is below 75mV in falling edge. DEM detection is suppressed during the ringing suppression time Tsupp (please refer to "**Ringing Suppression Timer**" section).

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2201. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state, the QR current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period.

- **Maximum and Minimum On-Time**

The minimum on-time of the system is determined by the LEB time (typical 300ns, RI=20K). The IC limits the on-time to a maximum time of 12.5uS.

- **Maximum Frequency Clamp**

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power decreases, the switching frequency can become rather high without limiting. To meet EMI limit and to achieve high efficiency at light loading conditions, the maximum switching frequency in OB2201 is internally limited to 90KHz.

- **Ringing Suppression Timer**

A ringing suppression timer Tsupp is implemented in OB2201. In normal operation, Tsupp starts when CS reaches the feedback voltage FB, the external power switch is set to off state. During Tsupp, the external power switch remains in off state and cannot be turned on gain. The ringing suppression time is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. In OB2201, the ringing suppression timer Tsupp is set to 2.5us internally.

- **OCP Compensation**

The variation of max output power in QR system can be rather large if no compensation is provided. The OCP threshold value is self adjusted lower at higher AC voltage. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage. In OB2201, a proprietary OCP compensation block is integrated and no external components are needed. The OCP threshold in OB2201 is a function of the switching ON time. For the ON time less than 12.5us, the OCP threshold changes linearly from 0.45V to 0.8V. For the ON time larger than 12.5us, the OCP threshold is clamped to 0.8V, as shown in Figure 3. (Note: RI=20K conditions)

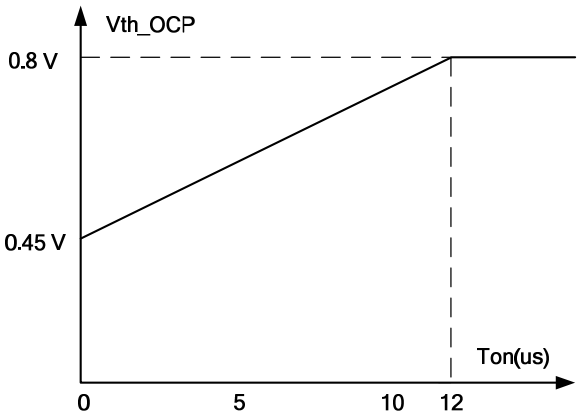


Figure 3

- **Adaptive Frequency Shuffling and Slope Compensation**

In OB2201, when the fix frequency CCM mode is touched, the frequency shuffling and slope compensation will be automatically added to the system to improve the EMI performance and current loop stability. The magnitude of shuffling

lies in the range of ±4% of 52K Hz. When the system leaves fix frequency CCM mode, the frequency shuffling and slope compensation will automatically disappear.

- **Output Over Voltage Protection (OVP)**

An output over voltage protection (OVP) is implemented by sensing the auxiliary winding voltage at DEM pin during the flyback phase. The auxiliary winding voltage is a well-defined replica of the output voltage. The OVP works by sampling the plateau voltage at DEM pin during the flyback phase. Internal 2.5us delay (plateau sensing) guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped.

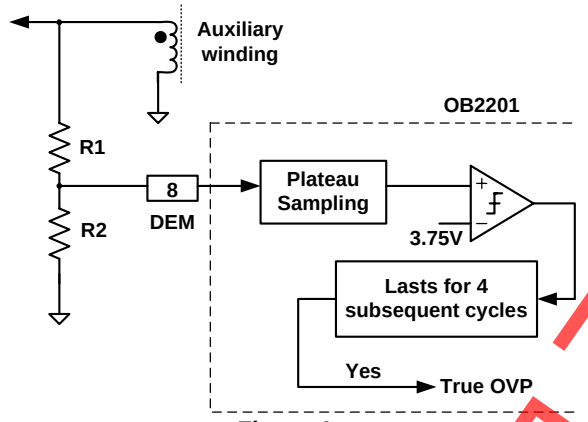


Figure 4

If the sampled plateau voltage exceeds the OVP trip level (3.75V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 4 cycles, the controller assumes a true OVP and it enters a latch off mode and stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level less than 4 successive cycles, the internal counter will be cleared and no fault is asserted.

- **Over Load Protection**

When over load (for example, short circuit) occurs, the feedback current of photo coupler is below minimum value, FB pin voltage approaches its floating pin voltage, then a fault is detected. If this fault is present for more than 80ms, the controller enters an auto-recovery soft burst mode. All pulses are stopped, VCC will drops below UVLO and the controller will try to restart with the power on soft start. It resumes operation once the fault disappears.

- **Over Temperature Protection with latch shutdown**

A NTC resistor in series with a regular resistor should be connected between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. A resistor between RI and GND sets internal reference current and the timer. The relationship between RT source current and RI resistor fellows below equation:

$$I\_RT = 100^* \frac{20K}{RI} \ (uA),$$

With 20K Ohm RI selected, an internal 100uA current flows through the NTC resistors. The voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shuts down the MOSFET when the sensed input voltage is lower than 1.05V. OTP is a latched shutdown.

- **Pin Floating and Short Protection**

OB2201 provides pin floating protection for RI, CS, FB, DEM, etc., and RI pin short protection. In cases when the pin are floating or RI pin is shorted to ground, Gate switching is disabled, thus protect the power system.

- **External latch trip point**

By externally forcing a level on pin RT (e.g.., with a signal coming from a temperature sensor) less than 1.05V, OB2201 can be permanently latched-off. To resume normal operation, VCC voltage should go below 6V (typical), which implies to unplug the SMPS from the mains.

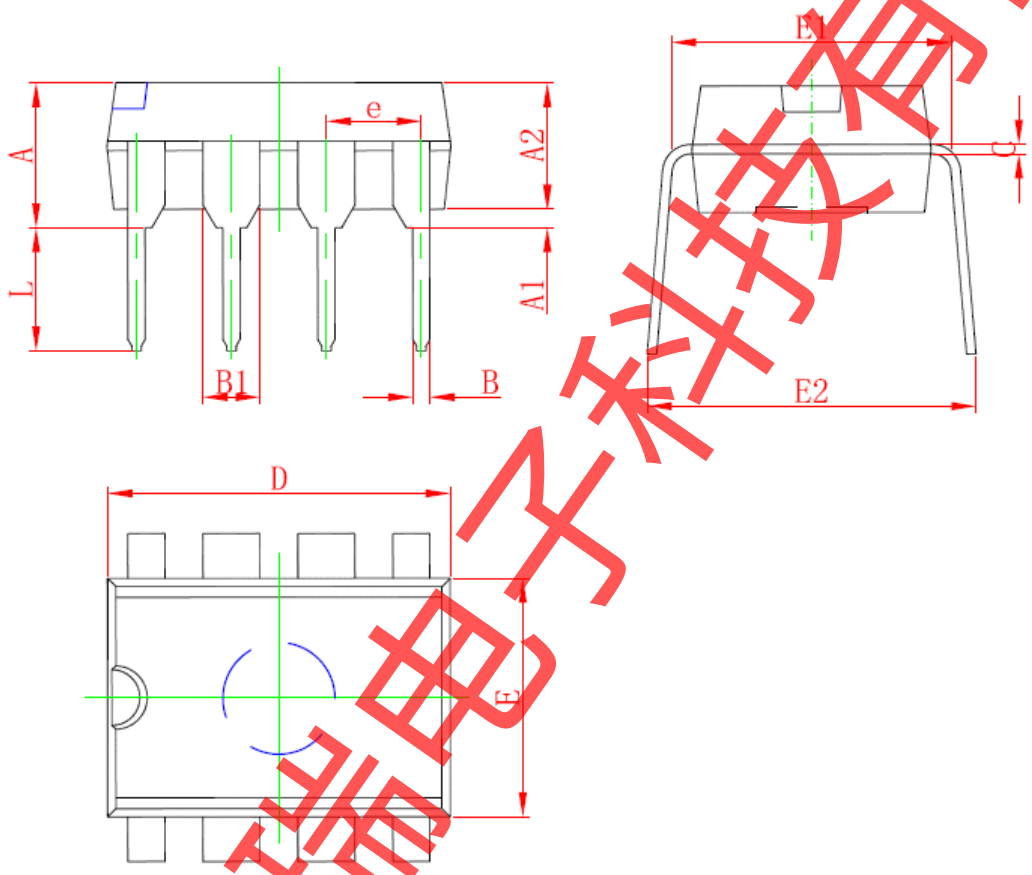
- **Gate Drive**

The Gate pin is connected to the gate of an external QR power switch with 0.8A capability. An internal 16.5V clamp is added for MOSFET gate protection at high VCC voltage. When VCC voltage drops below UVLO(ON), the Gate pin is internally pull low to maintain the off state.

PACKAGE MECHANICAL DATA

8-Pin Plastic DIP

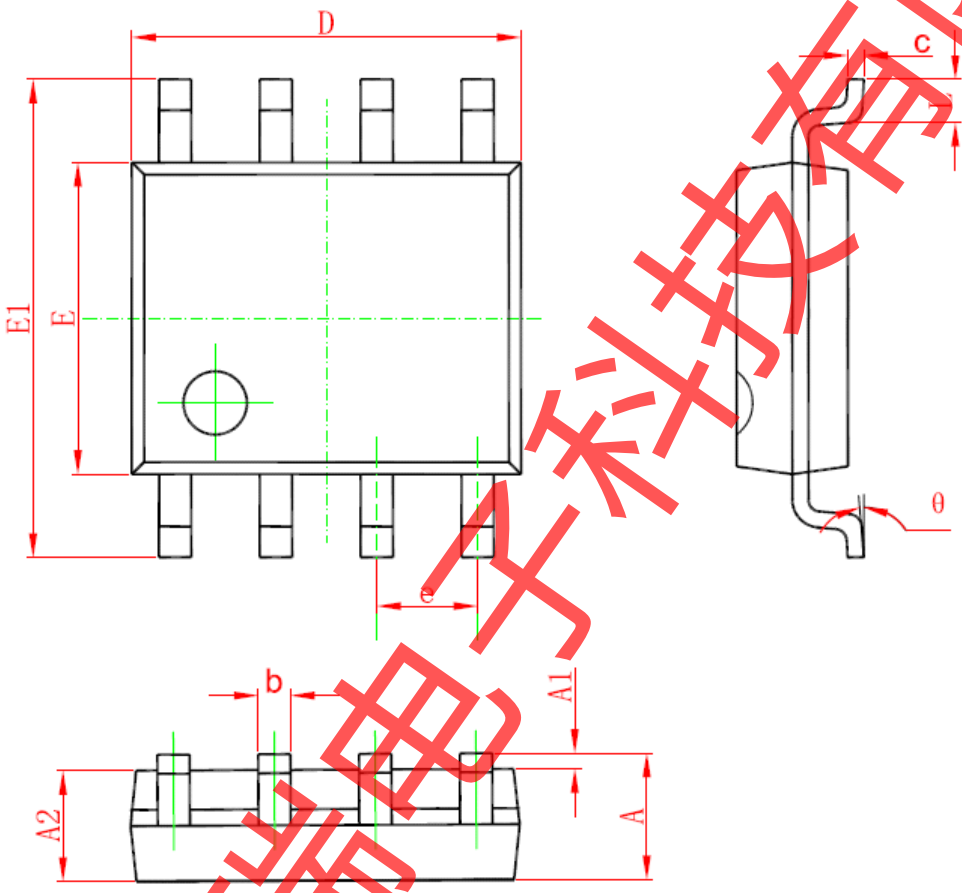
DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.21
A1	0.381		0.015	
A2	3.175	3.600	0.125	0.142
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.4
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.15
E2	8.200	9.525	0.323	0.375

8-Pin Plastic SOP

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

IMPORTANT NOTICE

RIGHT TO MAKE CHANGES

On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

WARRANTY INFORMATION

On-Bright Electronics Corp. warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent it deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

LIFE SUPPORT

On-Bright Electronics Corp.'s products are not designed to be used as components in devices intended to support or sustain human life. On-bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in medical applications.

MILITARY

On-Bright Electronics Corp.'s products are not designed for use in military applications. On-Bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in military applications.