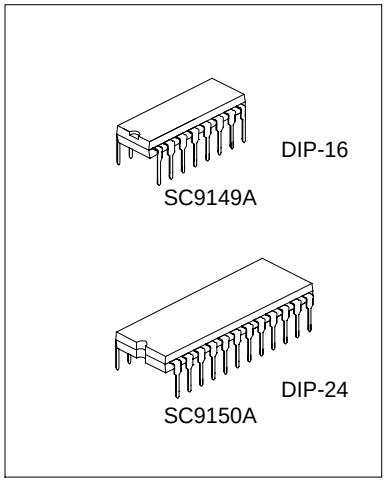
INFRARED REMOTE CONTROL RECEIVER



DESCRIPTION

The SC9149A/SC9150A are CMOS LSIs designed for use on the infrared remote control receiver, and when this LSI is used in combination with SC9148A for transmitter, the remote control system can be constructed. The SC9149A is DIP-16 type and is capable of controlling 10 functions, while the SC9150A is DIP-24 type and is capable of controlling 18 functions.

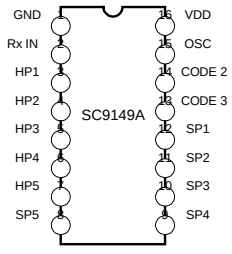
FEATURES

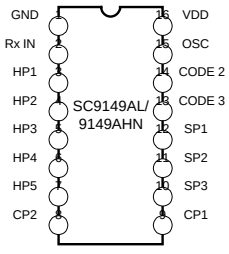
* Able to output parallel multiple keying signals sent from the transmitter (The SC9149A is able to output parallel up to 5 functions, while the SC9150A is able to output parallel up to 6 functions.)
* Output for single pulse, hold pulse and cyclic pulse are provided. (cyclic pulse is available only for SC9150A)
* A single terminal type oscillator by means of CR is provided.
* Code detection circuit provided for code check with the transmitter prevents inter-ferences from various types of machines and apparatus.

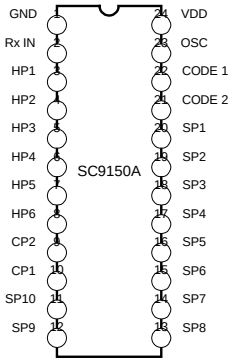
ORDERING INFORMATION

SC9149A	Advanced version DIP-16 package
SC9149AL	Advanced Dependent cyclic (toggle) Outputs
SC9149AHN	Inversed Rxin input Output format same as “L”, except that when HP1 or HP2 is active, it will clear CP1.
SC9150A	Advanced version DIP-24 package

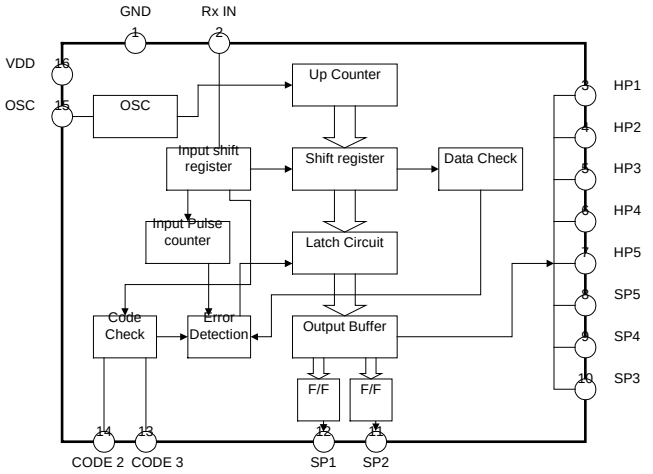
PIN CONFIGURATION



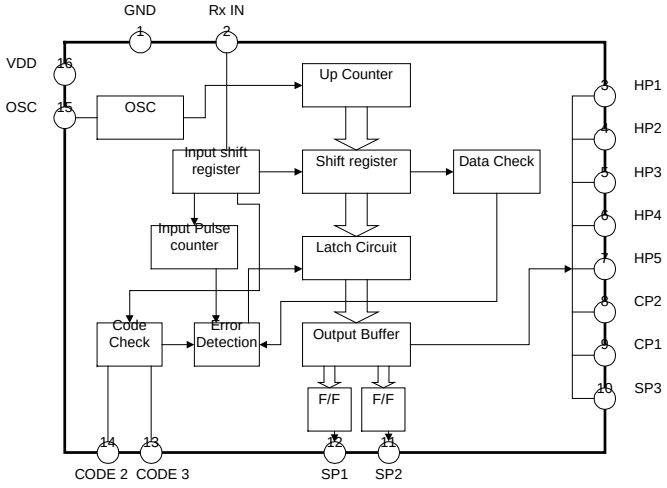




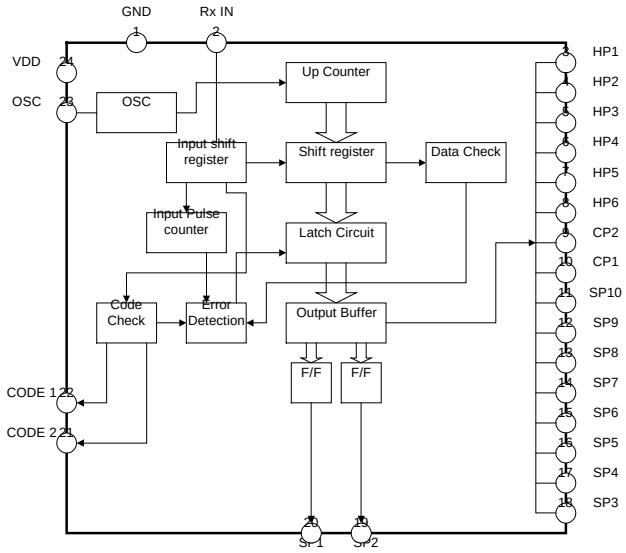
BLOCK DIAGRAM



SC9149A Block Diagram



SC9149AL/9149AHN Block Diagram



SC9150A Block Diagram

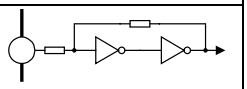
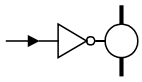
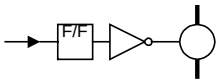
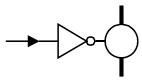
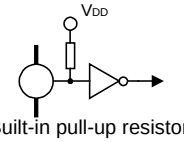
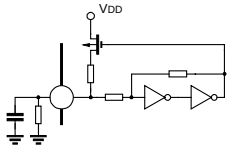
ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	0 ~ 6.0	V
Input / Output Voltage	V_{IN},V_{OUT}	Vss-0.3V ~ V_{DD}+0.3V	V
Power Dissipation	P_D	200	mW
Operating Temperature	Tamb	-20 ~ +75	°C
Storage Temperature	Tstg	-55 ~ +125	°C

ELECTRICAL CHARACTERISTICS(Tamb=25°C, V_{DD}=5.0V,Unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Supply Voltage		V_{DD}	Ta=25 ~ 75°C	4.5		5.5	V
Operating Supply Current		I_{DD}	Output without Load			1.0	mA
Standard OSC Frequency		Sfosc			38		kHz
Oscillation Frequency		fosc		27		57	kHz
Variance Of Oscillation Frequency By VDD		ΔV_{fosc}	V_{DD}=4.5~5.5V	-5		5	%
Variance Of Oscillation Frequency By Temperature		ΔT_{fosc}	Ta=-30~+75°C	-5		5	%
Output Current	"H" Level	I_{OH}	All output, V_{OH}=4.0V			-1.0	mA
	"L" Level	I_{OL}	All Output, V_{OL}=1V	1.0			mA
Input Current	"H" Level	I_{IH}	CODE Terminal, V_{IH}=5.0V	-1.0		1.0	µA
Pull-Up Resistor		Rup	CODE Terminal	10	20	40	kΩ
Input Circuit Threshold Voltage		V_{IN}	Rx Terminal	2.0	2.5	3.0	V
Hysteresis Width		V_{HIS}	Rx Terminal		0.8		V

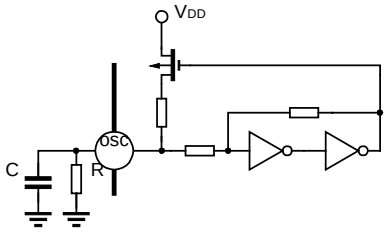
PIN DESCRIPTION

Pin No.			Symbol	Terminal	Function /operation	Input/output configuration
SC9149A	SC9149AL /9149AHN	SC9150A				
1	1	1	GND	GND		
2	2	2	Rx IN	Receiving signal input	Instruction signal with carrier signal eliminated is input.	
3~7	3~7	--	HP1 ~HP5	Continuous signal output	As long as receiving signal is input, this output is held at "H" level	
--	--	3~8	HP1 ~HP6			
--	9~8	9~10	CP1 ~CP2	Cyclic signal output	When receiving signal is input, output is reversed.	
--	12~10	--	SP1 ~SP3	Single-shot signal output	When receiving signal is input, output is placed at "H" level only for a fixed time.(about 107msec)	
8~12	--	--	SP1 ~SP5			
--	--	11~20	SP1 ~SP10			
13,14	13~14	21~22	CODE	Code input	Transmitter code is compared with a code set at this terminal and if they agree each other, input is accepted.	 Built-in pull-up resistor.
15	15	23	OSC	Timing oscillation	A resistor and a capacitor are parallel connected between this terminal and GND.	
16	16	24	V_{DD}	Power supply		

FUNCTIONAL DESCRIPTION

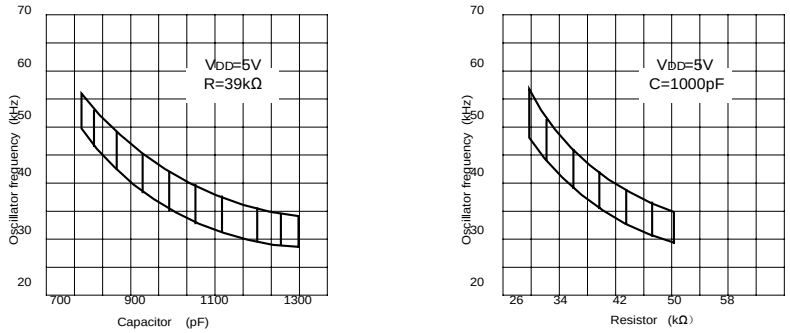
1. OSCILLATION CIRCUIT

Timing with transmitter signal and internal operating clock are all decided by this oscillator.

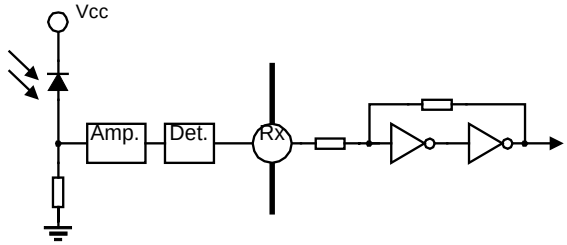


The oscillator has been so far constructed through a combination of a linear amplifier by means of CMOS inverter in IC and 455kHz ceramic resonator ;however , when SC9149A/SC9150A series are used , a stable oscillator can be constructed by parallel connecting C and R between the oscillator and GND by a single terminal oscillator . Oscillation frequency is about 38KHz±5 kHz at R=39kΩ and C=1000pF. (Refer to SCILLATION Frequency Characteristic below)

Oscillator frequency vs. resistor and capacitor



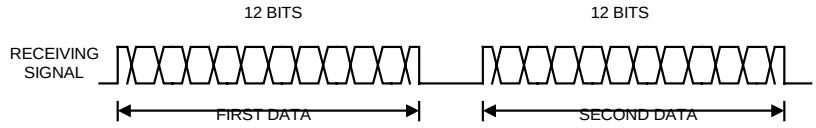
2. RECEIVING SIGNAL INPUT CIRCUIT



Signal received by the light receiving element is sent through the amplifier to the detector where 38 kHz carrier wave is eliminated and is input into the receiving signal input circuit . The receiving signal input circuit (Rx IN) has a built-in Schmitt circuit for shaping receiving signal waveform to eliminate rounding .

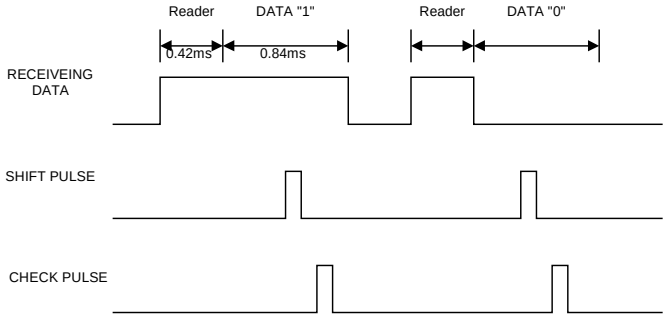
3. RECEIVING SIGNAL CHECK

The receiving signal check is to check 2 cycle transmitting signal sent from the transmitter to determine if it is normal signal .



First , the first data is stored in the 12-bits shift register. Then, when the second data is put into the shift register , data is forced out of the shift register by one bit , where the first data has been stored .

Now , pushed out data and incoming data to see if they are same . If an error is caused in the receiving data 12-bits check , the system is reset at that point of time . Conversely , when all receiving data are OK , output is raised from "L" level to "H" level .



The status of receiving data , shift pulse and check pulse is shown above . Shift pulse is provided in the data center by taking frequency margins of the transmitter and the receiver into consideration .

4.Code Comparison

To prevent interference with other models , C1, C2 and C3 code bits are provided for checking whether the transmitter and receiver codes agree each other .

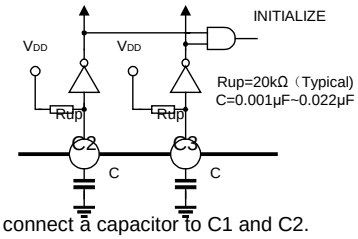
Only when both codes agreed , internal latch strobe pulse is generated to latch receiving data and output is raised from 'L" level . if both codes do not agree , no latch strobe pulse is generated and output remains at "L" level .

Code bits used differ depending upon receiver as shown below :

CODE BIT		
C1	C2	C2,C3 are used for SC9149A/9149AL/9149AHN C1,C2 are used for SC9150A. Code bit “0”, “0” can not be used.
C3	C2	
1	0	
0	1	
1	1	

5.INITIALIZATION

In order to initialize the internal status at time of power ON, it is necessary to perform the initialization. The initialization is carried out when a capacitor is connected to the code bit terminal.

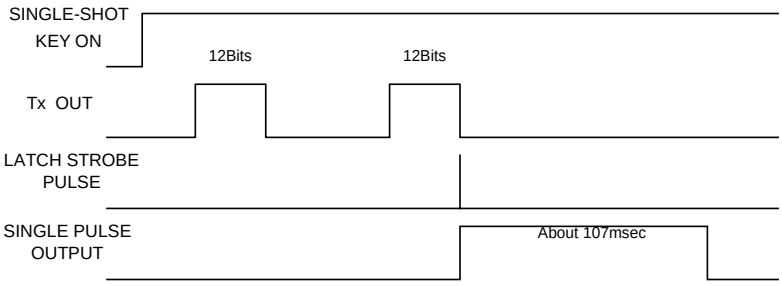


NOTE: * In case of SC9149A series, connect a capacitor to C1 and C2.

* A capacitor for initialization is unnecessary for the terminal for which code bit "0" is selected. However, code bit "0", "0" can not be used. Either one terminal must be set at "H".

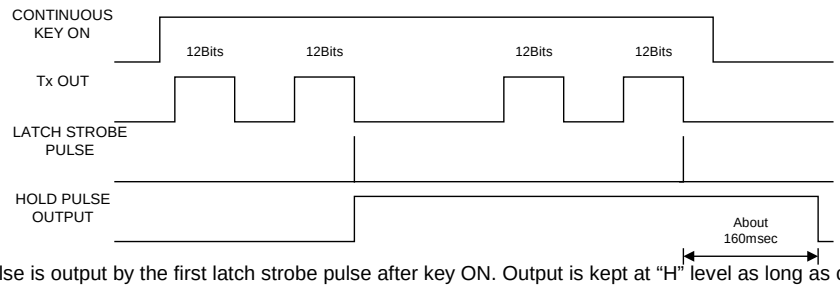
6. EXPLANATION OF OUTPUT PULSE SP,HP,CP

6-1. SP1~SP5 (SINGLE PULSE)



After checking 12-bits receiving data, if data agree and OK, single pulse is output.
Output is raised from "L" level to "H" level and returned again to "L" level after about 107msec.

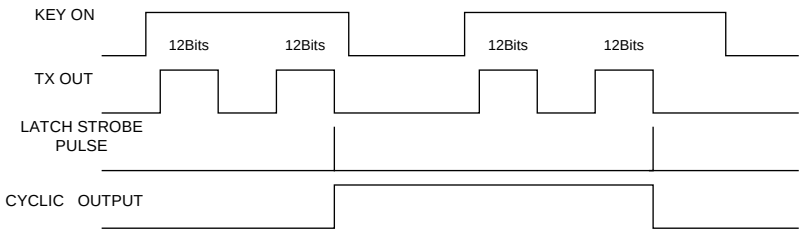
6-2. HP1~HP5 (Hold pulse)



Hold pulse is output by the first latch strobe pulse after key ON. Output is kept at "H" level as long as continuous signal is Input. When the key is released and continuous signal is stopped, about 160msec later, output is reversed to "L" by the last latch strobe pulse. Further, HP1~HP5 are able to parallely and simultaneously maximum sextet outputs at "H" level by continuous signal sent from the transmitter.

These outputs are optimum as outputs of REC-PLAY,REC-PAUSE, and CUE/REVIEW of tape deck.

6-3. CP1,CP2 (Cyclic Pulse)



When single-shot signal received, cyclic pulse output is reversed. This cyclic pulse is used for power ON/OFF, MUTE etc.

7.CODE ALLOCATION (KEY NO. IS FOR SC9148A)

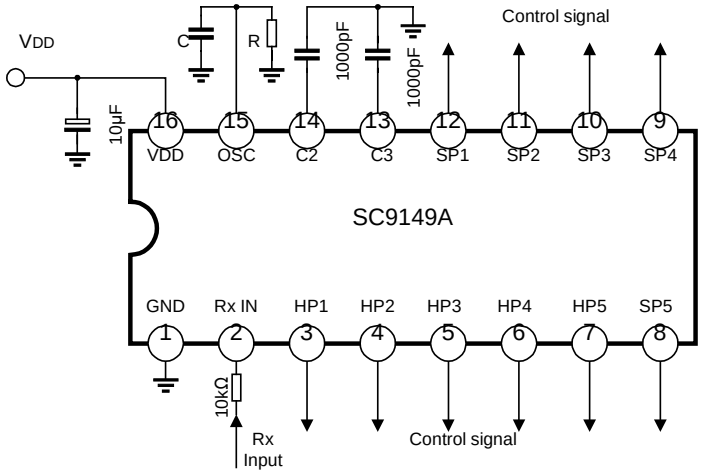
Key No.	DATA BIT									FUNCTION OF INSTRUCTION	
	H	S1	S2	K1	K2	K3	K4	K5	K6		
1	1	0	0	1	0	0	0	0	0	Continuous Signal	HP1
2	1	0	0	0	1	0	0	0	0	Continuous Signal	HP2
3	1	0	0	0	0	1	0	0	0	Continuous Signal	HP3
4	1	0	0	0	0	0	1	0	0	Continuous Signal	HP4
5	1	0	0	0	0	0	0	1	0	Continuous Signal	HP5
6	1	0	0	0	0	0	0	0	1	Continuous Signal	HP6
7	0	1	0	1	0	0	0	0	0	Single-shot signal	SP1
8	0	1	0	0	1	0	0	0	0	Single-shot signal	SP2
9	0	1	0	0	0	1	0	0	0	Single-shot signal	SP3
10	0	1	0	0	0	0	1	0	0	Single-shot signal	SP4
11	0	1	0	0	0	0	0	1	0	Single-shot signal	SP5
12	0	1	0	0	0	0	0	0	1	Single-shot signal	SP6
13	0	0	1	1	0	0	0	0	0	Single-shot signal	SP7
14	0	0	1	0	1	0	0	0	0	Single-shot signal	SP8
15	0	0	1	0	0	1	0	0	0	Single-shot signal	SP9
16	0	0	1	0	0	0	1	0	0	Single-shot signal	SP10
17	0	0	1	0	0	0	0	1	0	Cyclic Signal	CP1
18	0	0	1	0	0	0	0	0	1	Cyclic Signal	CP2

C1~C3 code bits are available in addition to the above data bits for optional selection.

SC9150A can use all keys, but SC9149A is able to use KEY1~5 and KEY 7~11 only for 10 commands. SC9149AL/9149AHN is able to use KEY1~5 and KEY 7~9, KEY 17~18 only for 10 commands.

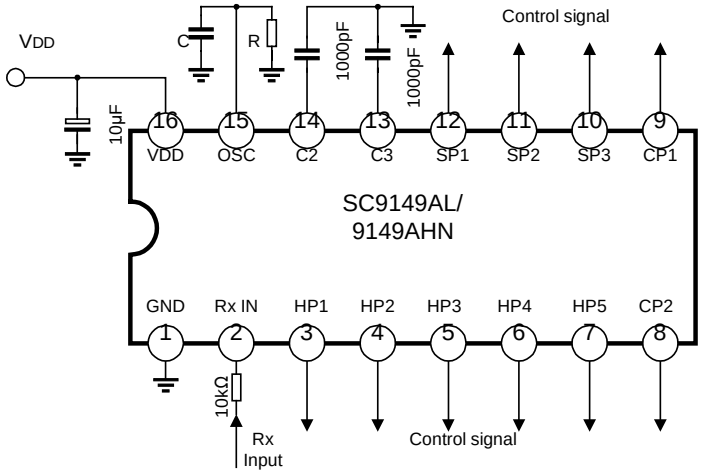
TYPICAL APPLICATION CIRCUIT

1. SC9149A CIRCUIT



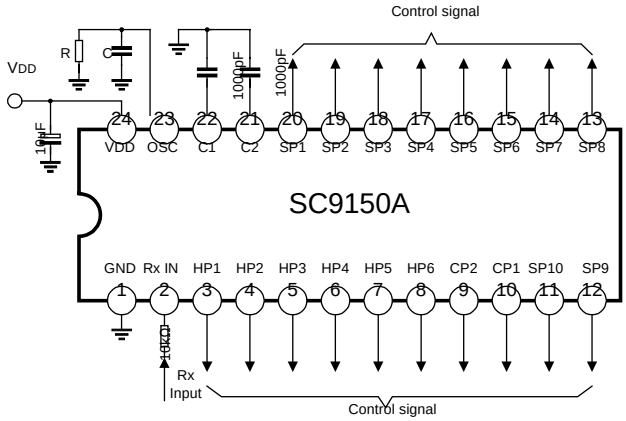
R should be 38kΩ±5%
C should be polypropylene film capacitor having good temperature characteristics 1000pF±5%.

2. SC9149AL/9149AHN CIRCUIT



R should be 38kΩ±5%
C should be polypropylene film capacitor having good temperature characteristics 1000pF±5%.

3. SC9150A CIRCUIT

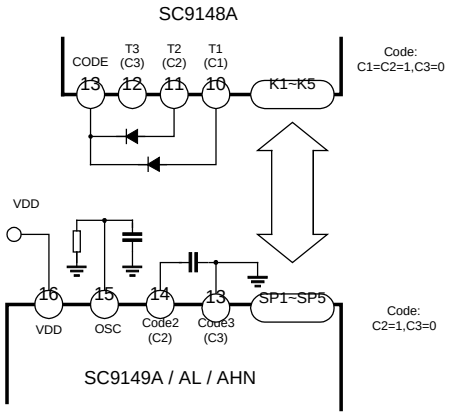


R should be 38kΩ±5%.

C should be polypropylene film capacitor having good temperature characteristics 1000pF±5%.

NOTE FOR APPLICATION CIRCUIT

1. COMBINATION OF SC9148A/SC9149A / AL / AHN CODE BITS



Example 1 (C2=1 and C3=0)

The combination of code bits of SC9148A and SC9149A is shown in the following table.

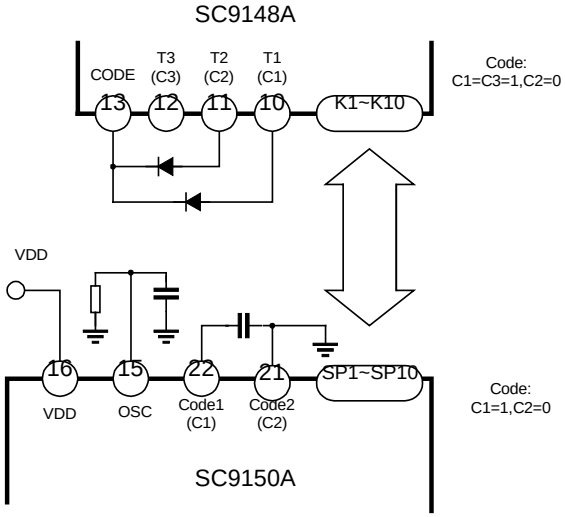
SC9148A			SC9149A / AL / AHN	
C1	C2	C3	C2	C3
1	1	0	1	0
1	0	1	0	1
1	1	1	1	1

To make code bit to “1” on SC9148A, connect diode to CODE terminal from T1~T3 terminal. To set Code bit “0” , open the circuit.

SC9149A has C2 and C3 code terminal. Code bit of C1 has been pulled up in IC and C1 is always kept at “1” status.

Therefore, on transmitter SC9148A it is necessary to keep C1 code bit at “1” . Example 1 is the external circuit diagram when Code bit C2=1 and C3=0.

2. COMBINATION OF SC9148A/SC9150A CODE BITS



Example 2 (C1=1 and C2=0)

The combination of code bits of SC9148A and SC9150A is shown in the following table.

SC9148A			SC9150A	
C1	**C2**	**C3**	**C2**	**C3**
1	0	1	1	0
0	1	1	0	1
1	1	1	1	1

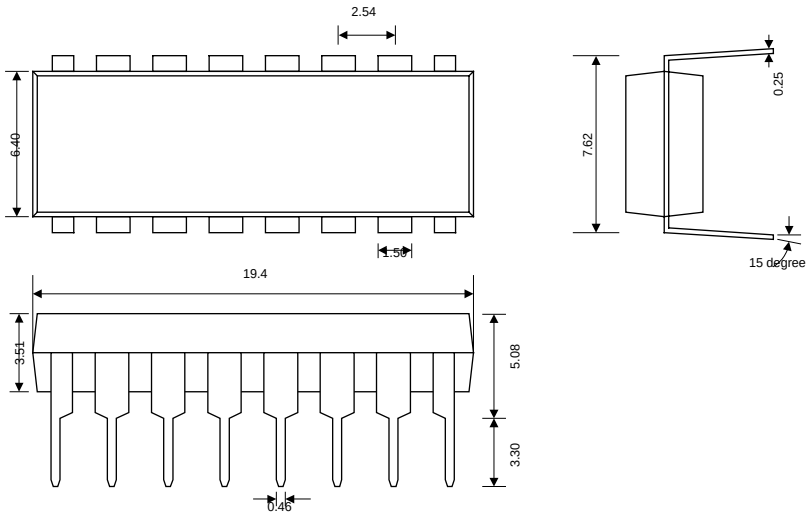
On SC9150A, C3 code has been pulled up in IC and always kept at “1” status. Therefore , it is necessary to keep Code Bit C3 of transmitter SC9148A at “1”. To keep Code Bit C3 at “1”, connect a diode to CODE terminal from T3 terminal.

4. Note for Input Signal

If input voltage above VDD+0.3V may possibly be applied to Rx Input Terminal(2 Pin), connect resistor of about 10kΩ in series to Rx Input terminal in order to prevent latch-up.

PACKAGE OUTLINE

DIP-16-300-2.54 UNIT:mm



DIP-24-600-2.54 UNIT:mm