DATA SHEET

(DOC No. HX8861-H11-DS)

HX8861-H11

TFT LCD Timing controller
with LVDS input and
mini-LVDS output

Version 03 May, 2014

Himax Technologies, Inc.
http://www.himax.com.tw

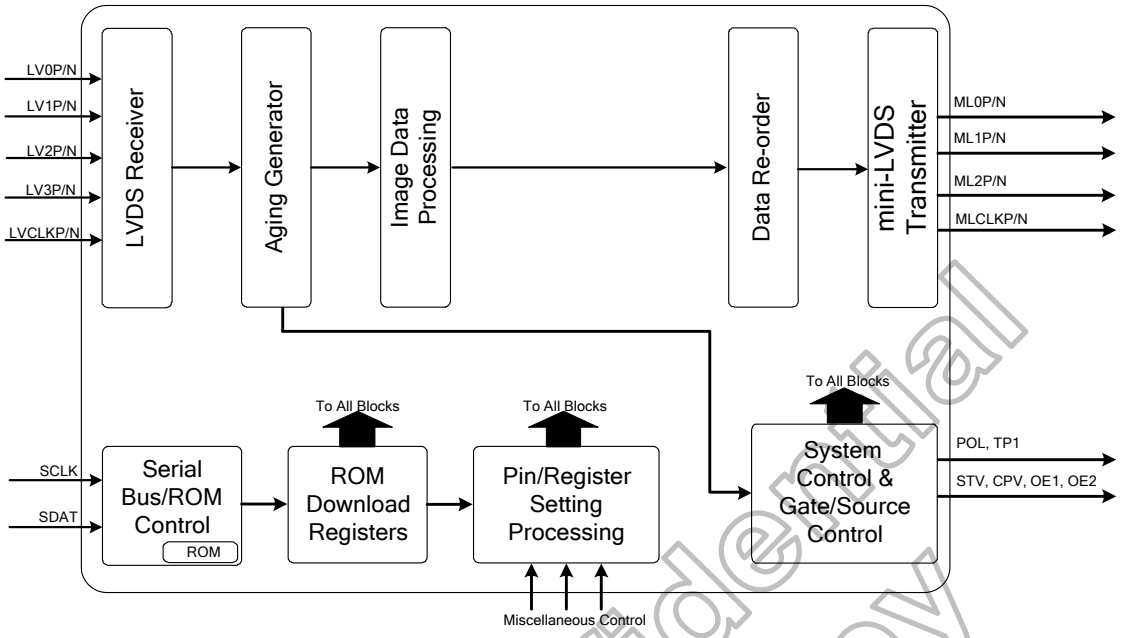
1. General Description

The HX8861-H11 is a timing controller embedded with a single pixel LVDS receiver and a 3-pair mini-LVDS transmitter for TFT LCD panel. The mini-LVDS is a low EMI and low voltage swing interface that transmits data between the timing controller and source drivers. The HX8861-H11 supports WXGA **(1366X768)** and other resolutions with EEPROM.

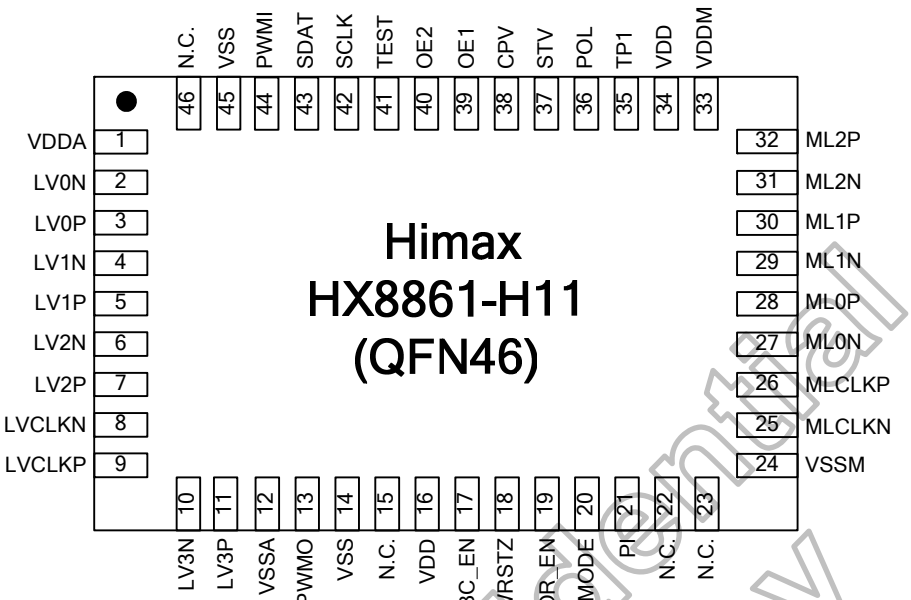
2. Features

- Input frequency range from 25MHz to 110MHz
- mini-LVDS frequency range from 50MHz to 300MHz
- Support WXGA **(1366X768)** and other resolutions with EEPROM
- Built-in single pixel LVDS receiver
- Built-in mini-LVDS transmitter for low power consumption and low EMI
- Built-in single port 6-bit mini-LVDS 3-pair differential bus interface output
- Support both 6/8 bit inputs. 8-bit input and 6-bit output with FRC mode **(16.7M colors)**
- Embedded with aging generator for simplifying TFT LCD panel dynamic burn-in test
- Support DE mode only
- Support serial bus programming
- Support dual-gate panel structure
- Support gamma correction function
- Support POL 1, $1+2^n$, 2^n, $2+2^n$ **(n=1 ~ 8)** line, column inversion by ROM code setting
- Support LVDS input port mirror function by ROM code setting
- Support LVDS VESA/JEIDA format by ROM code setting
- Support mini-LVDS output skew control with EEPROM
- Support CE **(hue/saturation, brightness/contrast, sharpness adjustment)** function
- Support CABC **(Content Adaptive Brightness Control)** function
- Support SDRRS **(Seamless Dynamic Refresh Rate Switching)** function
- Support 5V tolerance input pads: CABC_EN, COLOR_EN, AGMODE, PWMI
- Supply voltage: VDD=2.5V/3.3V **(2.3V~3.6V)**
- 46-pin QFN package with E-PAD
- HX8861-H11DDKG: support ≧ 32K bit EEPROM only
- HX8861-H11DDKG-E: support 2K to 16K bit EEPROM only

3. Block Diagram



4. Pin Assignment



5. Pin Description

Pin name	Pin no.	I/O	Description
LVDS input signals			
LV0P/N LV1P/N LV2P/N LV3P/N	3,2 5,4 7,6 11,10	In	LVDS differential data pairs.
LVCLKP/N	9,8	In	LVDS differential clock pairs.
mini-LVDS output signals			
ML0P/N ML1P/N ML2P/N	28,27 30,29 32,31	Out	mini-LVDS outputs to source drivers.
MLCLKP/N	26,25	Out	mini-LVDS clock outputs to source drivers.
PI	21	In	External resistor input for mini-LVDS output swing control.
Gate/Source driver control signals-for normal or dual-gate mode			
N.C.	15,22 23,46	Out	No connection pin. It should be floating.
TP1	35	Out	Data latch output to source driver.
POL	36	Out	Polarity inversion output to source driver.
STV	37	Out	Start pulse to gate driver.
CPV	38	Out	Gate driver clock.
OE1	39	Out	Output enable signal to gate driver.
OE2	40	Out	Gate pulse modulation signal.
Miscellaneous control signals			
PWMO	13	Out	Backlight control output.
CABC_EN(1)	17	In	CABC function selection, default CABC_EN=L. CABC_EN=H: Enable CABC function. CABC_EN=L: Disable CABC function.
/HWRSTZ	18	In	Reset input **(low active)**.
COLOR_EN(1)	19	In	Color engine function selection, default COLOR_EN=L. COLOR_EN=H: Enable color engine function. COLOR_EN=L: Disable color engine function.
AGMODE(1)	20	In	Aging pattern selection, default AGMODE=L. AGMODE=H and no clock in: BIST pattern. AGMODE=L and no clock in: Black pattern.
TEST	41	In	Test mode selection, default TEST=L. TEST=H: Test mode. TEST=L: Normal operation.
SCLK	42	In/Out	Control register input clock **(using EEPROM)**.
SDAT	43	In/Out	Control register input data **(using EEPROM)**.
PWMI(1)	44	In	Backlight control input.
Power supply			
VDD	16,34	In	Digital power supply.
VDDA	1	In	Power supply for analog.
VDDM	33	In	mini-LVDS power supply.
VSS	14,45	In	Grounding for VDD.
VSSA	12	In	Grounding for VDDA.
VSSM	24	In	Grounding for VDDM.
E-Pad	-	-	Exposed pad is connected to VSS internally, the soldering coverage rate should be over 75%.

Note: (1) 5V tolerance input pads.

6. Function Description

6.1 LVDS receiver

The HX8861-H11 has a built-in single pixel LVDS receiver that converts data from differential serialized format to parallel output.

Ideal strobe position for LVDS input

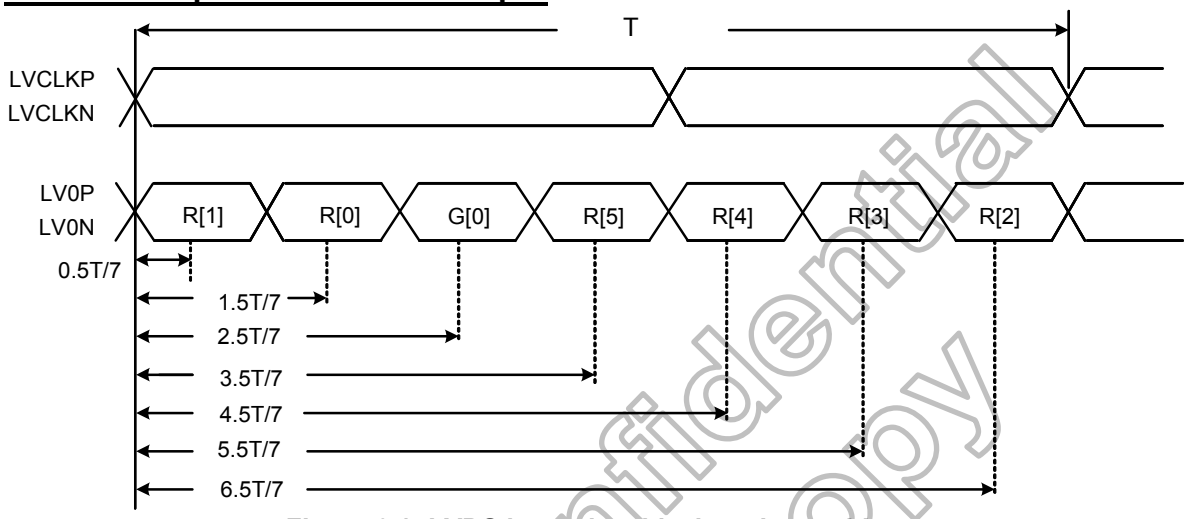


Figure 6.1: LVDS input data ideal strobe position

LVDS input data mapping

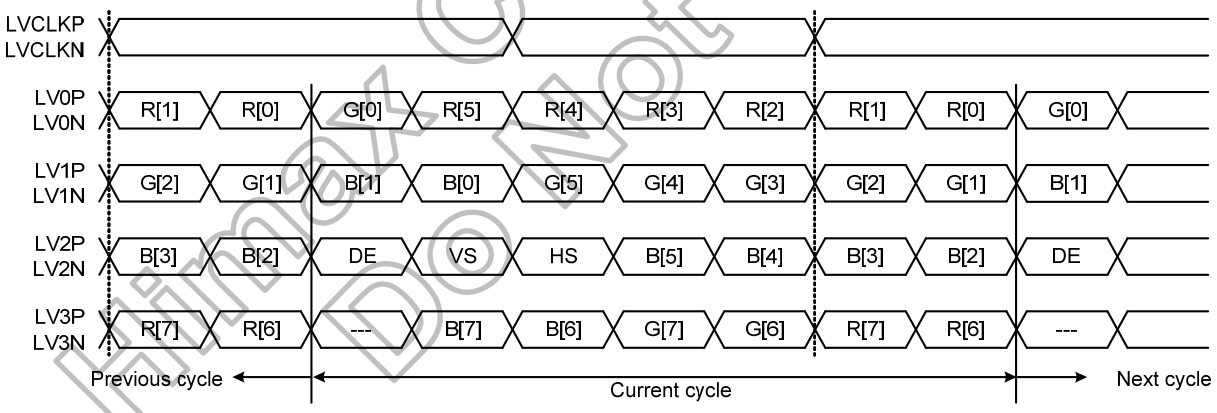


Figure 6.2: LVDS input data mapping (VESA format)

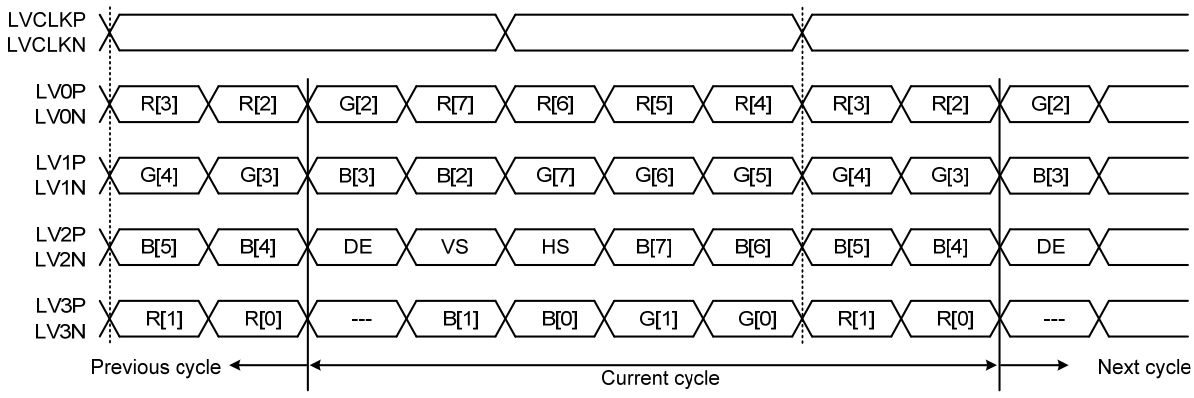


Figure 6.3: LVDS input data mapping (JEIDA format)

6.2 Aging function

The HX8861-H11 is embedded with an aging generator for simplifying TFT LCD model dynamic burn-in test. When AGMODE pin is pulled to VDD and no clock is detected, the HX8861-H11 will operate at aging mode and generate BIST **(Built-In Self Test)** patterns as Figure 6.4. When AGMODE pin is low or open, and no clock is detected, the HX8861-H11 will generate black pattern.

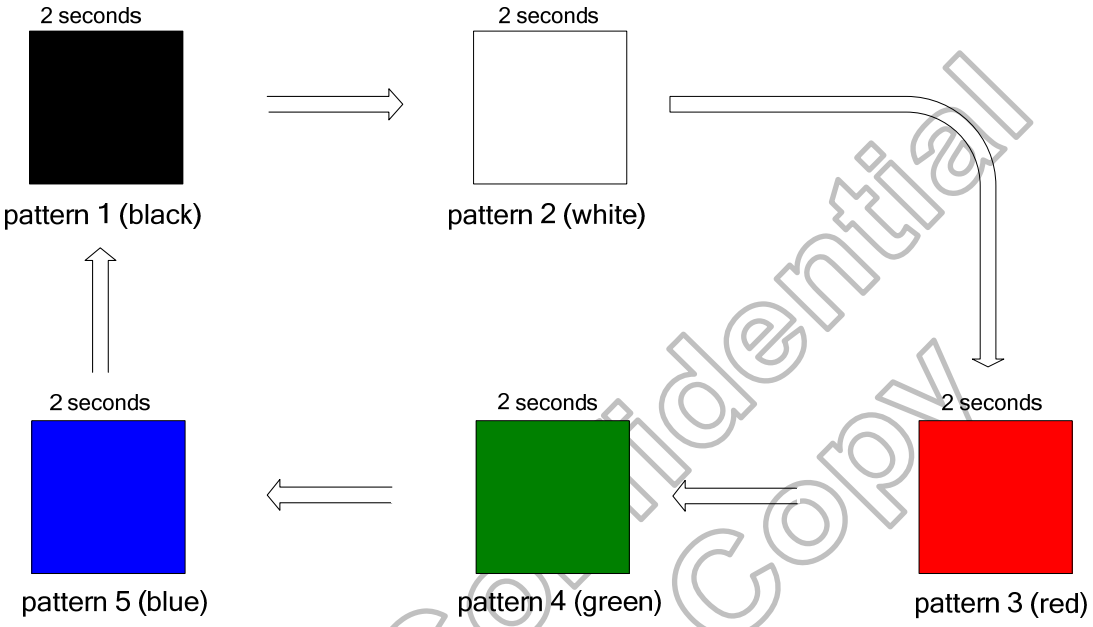


Figure 6.4: BIST patterns

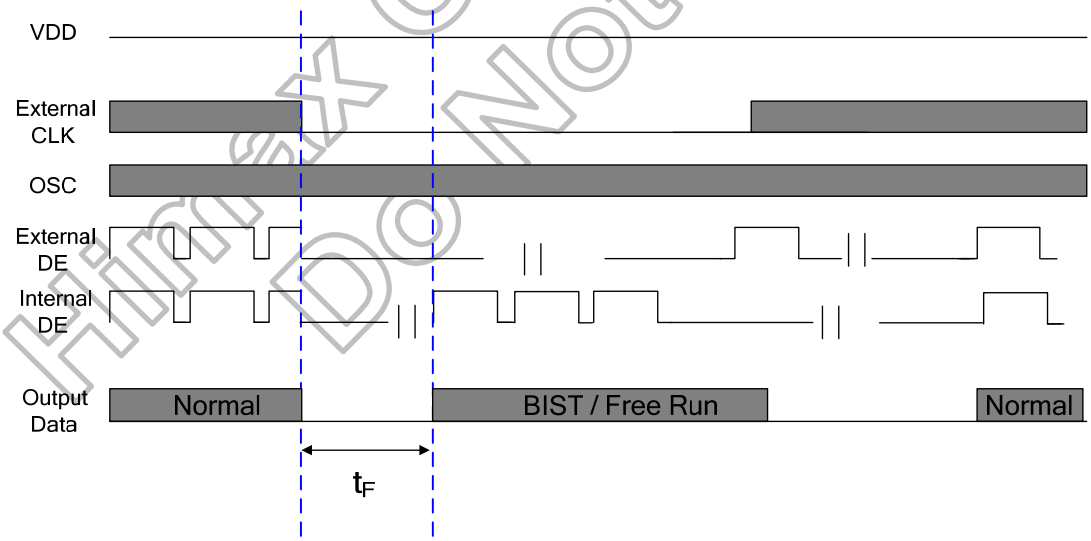


Figure 6.5: Free run timing

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
t_F	Detection time	50	-	100	ms

6.3 Serial bus configuration

The HX8861-H11 can easily adjust parameter by serial bus including source/gate control timing, output data mapping, etc.

6.4 CABC function

The CABC function generates a PWM signal to control backlight modulation. The duty ratio of PWM is generated by image histogram and works with gamma correction. PWMO frequency will follow PWMI frequency when PWMI is a modulation signal. PWMO frequency can generate specific frequency **(refer to below table)** by internal setting if the PWMI is DC level.

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
F_I	Backlight control input Frequency	CABC Enable/Disable	100	-	30K	Hz
D_I	Backlight control input Duty	CABC Enable/Disable	1	-	100	%
F_O	Backlight control output Frequency	CABC Disable	100	-	30K(1) STV*$2^{n(2)}$	Hz
		CABC Enable	100	-	STV*$2^{n(2)}$ 100K(3) 30K(4)	Hz
D_O	Backlight control output Duty	CABC Disable	1	-	100	%

Note: (1) PWMO frequency will follow PWMI
(2) PWMO is the multiple of STV frequency **(n=0~10, n is integer)** and independent of PWMI.
(3) When PWMI frequency is always DC level.
(4) When PWMI frequency is not DC level and PWMO frequency will follow PWMI.

6.5 Color engine function

The HX8861-H11 with color engine IP can support hue/saturation, brightness/ contrast, sharpness adjustment function.

6.6 Gate/source control timing

The HX8861-H11 generates control signals for source and gate drivers according to the settings in EEPROM. Examples of timing specifications are shown as below.

Description	Symbol	WXGA	Unit
Reset pulse leading to TP1	td1	2064	mini-LVDS Clock
High duration of TP1	tw1	99	mini-LVDS Clock
Reset pulse leading to POL **(1+2 line)**	td2	900	mini-LVDS Clock
High/Low duration of POL **(1+2 line)**	tw2	2	Line
Reset pulse leading to CPV rising	td3	2064	mini-LVDS Clock
High duration of CPV	tw3	1167	mini-LVDS Clock
Reset pulse leading to STV rising	td4	900	mini-LVDS Clock
High duration of STV	tw4	1	Line
Reset pulse leading to OE1/OE2 rising	td5	1728/1389	mini-LVDS Clock
High duration of OE1/OE2	tw5	450/429	mini-LVDS Clock

Note: (1) The timing can be customized by different panel characteristics through ROM code.

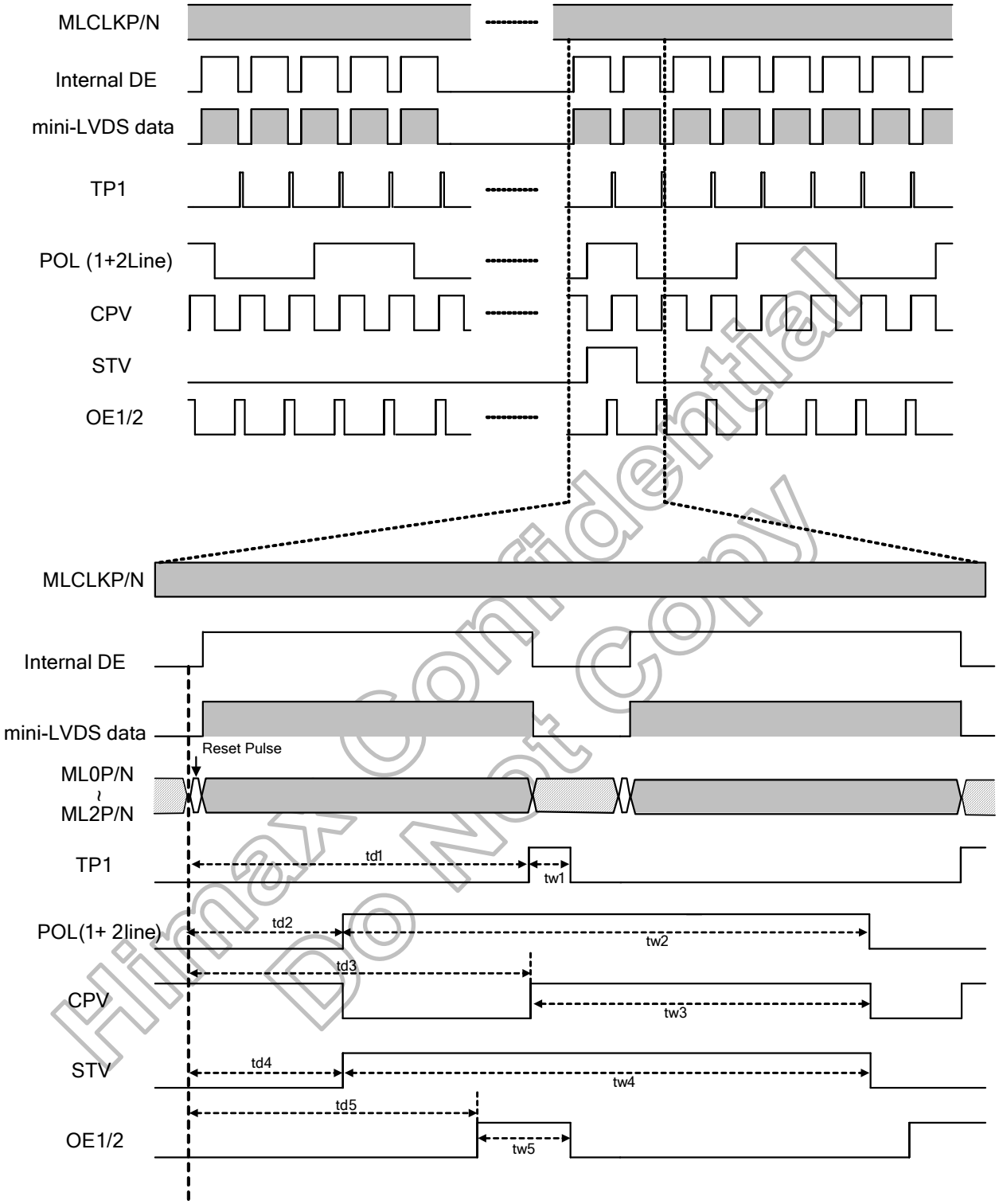


Figure 6.6: Control signal output timing characteristic

6.7 POL inversion

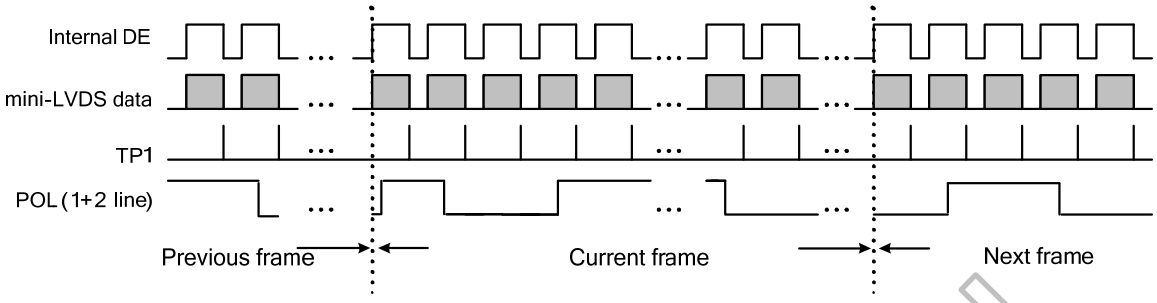


Figure 6.7: POL 1+2 line frame inversion

6.8 Input signal timing

Parameter	Symbol	Condition	WXGA	Unit
Horizontal total timing	HT	Min.	1420	Clock
		Typ.	1526	Clock
		Max.	2047	Clock
Horizontal active timing	HVD	Typ.	1366	Clock
Vertical total timing	VT	Min.	771	Line
		Typ.	790	Line
		Max.	2047	Line
Vertical active timing	VVD	Typ.	768	Line

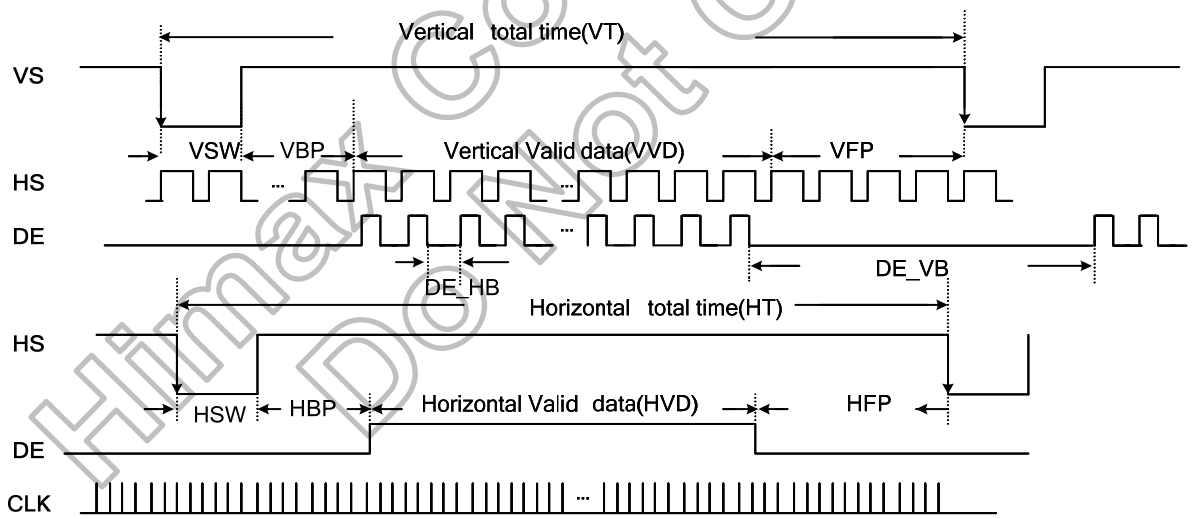


Figure 6.8: Input video signal format

6.9 Seamless Dynamic Refresh Rate Switching (SDRRS)

Seamless Dynamic Refresh Rate Switching **(SDRRS)** is a power saving technology that lowers the pixel clock frequency and frame rate to TFT LCD in response to power policy, and display activity. The HX8861-H11 will detect the loss of signals and drive the panel into a safe refresh mode. As a result of the actions of the HX8861-H11, the switch between refresh rates will not cause a noticeable impact on display quality.

SDRRS response time

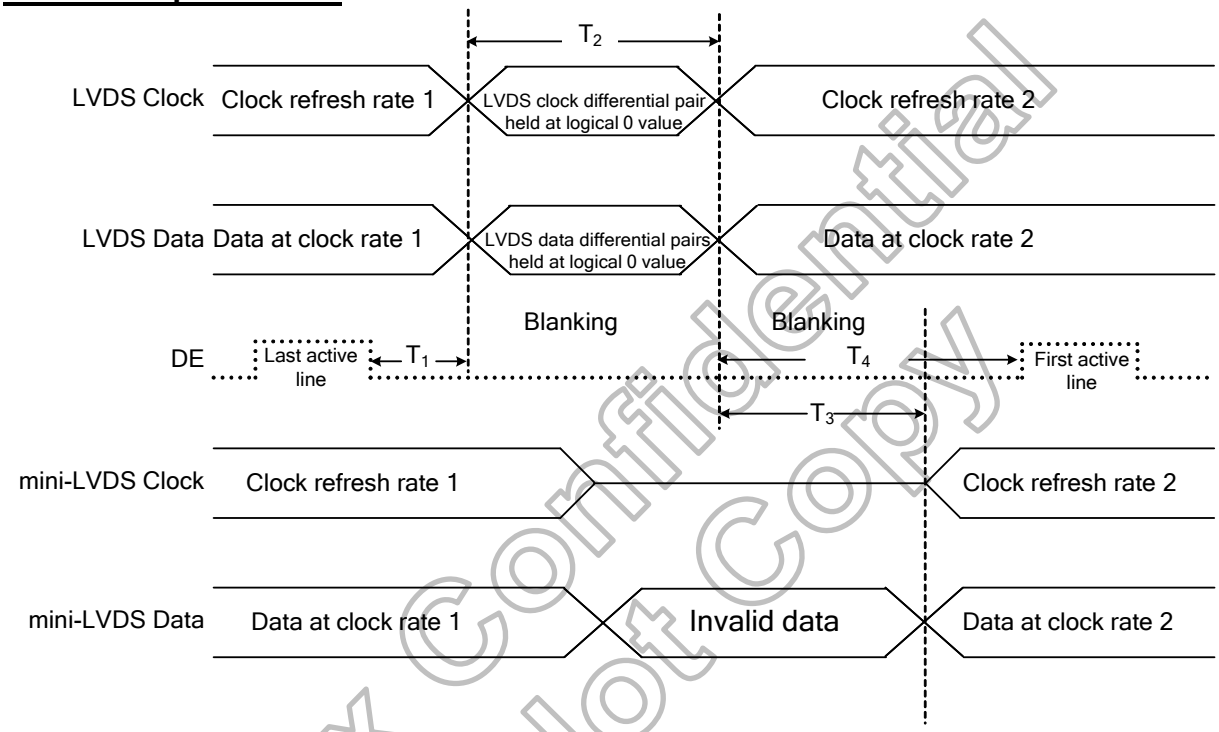


Figure 6.9: TCON receive lock time at switching refresh rates

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
T_1	VBlank at refresh rate 1	2	-	3	Line
T_2	LVDS clock differential pair held at logical 0 value	50	-	100	µs
T_3	TCON receive lock time	-	-	200	µs
T_4	Refresh rate 2 to first active line	200	-	-	µs

6.10 Spread Spectrum Clock Generator (SSCG)

The SSCG function is used for reducing EMI. The modulation of SSCG IP is symmetrically centered and triangular on the output frequency. The specifications are detailed listed at section 8.4.

6.11 EEPROM mapping memory

6.11.1 TCON only: 4K bit memory space

Block Address	000	001
Word Address	00---FF	00---FF
Function	Timing	Timing

6.11.2 TCON + color engine: 6K bit memory space

Block Address	000	001	010
Word Address	00---FF	00---FF	00---FF
Function	Timing	Timing	Color engine

6.11.3 TCON + CABC: 8K bit memory space

Block Address	000	001	010	011
Word Address	00---FF	00---FF	00---FF	00---FF
Function	Timing	Timing	CABC	

6.11.4 TCON + CABC + color engine: 10K bit memory space

Block Address	000	001	010	011	100
Word Address	00---FF	00---FF	00---FF	00---FF	00---FF
Function	Timing	Timing	Color engine	CABC	

6.11.5 TCON + DGC: 10K bit memory space

Block Address	000	001	010	011	100
Word Address	00---FF	00---FF	00---FF	00---FF	00-00---FF F
Function	Timing	Timing	Red Gamma (DGC)	Green Gamma (DGC)	Blue Gamma (DGC)

6.11.6 TCON + color engine + DGC: 12K bit memory space

Block Address	000	001	010	011	100	101
Word Address	00---FF	00---FF	00---FF	00---FF	00---FF	00---FF
Function	Timing	Timing	Color engine	Red Gamma (DGC)	Green Gamma (DGC)	Blue Gamma (DGC)

6.11.7 TCON + DGC + CABC: 14K bit memory space

Block Address	000	001	010	011	100	101	110
Word Address	00---FF	00---FF	00---FF	00---FF	00-00---FF F	00---FF	00---FF
Function	Timing	Timing	Red Gamma (DGC)	Green Gamma (DGC)	Blue Gamma (DGC)	CABC	

6.11.8 TCON + color engine + DGC + CABC: 16K bit memory space

Block Address	000	001	010	011	100	101	110	111
Word Address	00---FF	00---FF	00---FF	00---FF	00---FF	00---FF	00---FF	00---FF
Function	Timing	Timing	Color engine	Red Gamma (DGC)	Green Gamma (DGC)	Blue Gamma (DGC)	CABC	

7. DC Characteristics

7.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	VDD	-0.3	-	+4.0	V
CMOS/TTL input voltage	V_{IN}	-0.3	-	VDD	V
CMOS/TTL output voltage	V_{OUT}	-0.3	-	VDD	V
LVDS receiver input voltage	V_{IN}	-0.3	-	VDD	V
Storage temperature	T_{STG}	-40	-	125	℃
Junction temperature	T_J	-	-	125	℃
Thermal resistance **(junction ambient)**	Θ_{JA}	-	-	100(1)	℃/W

Note: (1) For 2-layer standard JEDEC PCB.

7.2 Recommended operating conditions

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	VDD	3.0(1)	3.3(1)	3.6(1)	V
		2.3(2)	2.5(2)	2.7(2)	V
Operating temperature	T_A	0	25	70	℃
LVDS receiver input voltage	V_{IN}	0	-	2.4	V

Note: (1) For +3.3V operation.
(2) For +2.5V operation.

7.3 DC electrical characteristics

Symbol	Parameter		Condition	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
I_{DD}	Supply current		F=75MHz, PI=14KΩ, RL=100Ω pixel checker pattern	-	54	-	mA
CMOS/TTL DC Specifications							
V_{IH}	High level input voltage		-	0.7VDD	-	VDD	V
V_{IL}	Low level input voltage		-	VSS	-	0.3VDD	V
V_{OH}	High level output voltage		-	0.8VDD	-	VDD	V
V_{OL}	Low level output voltage		-	VSS	-	0.2VDD	V
I_{IN}	Input current		-	-10	-	10	μA
R_{PD}	Pull low resistance	VDD=3.3V	CABC_EN **(Pin 17)** COLOR_EN **(Pin 19)** AGMODE **(Pin 20)** TEST **(Pin 41)** PWMI **(Pin 44)**	50	100	150	KΩ
		VDD=2.5V		75	150	225	KΩ
LVDS DC Specifications							
V_{TH}	Differential input high threshold		V_{IC}=1.2V	-	-	+100	mV
V_{TL}	Differential input low threshold			-100	-	-	mV
V_{IC}	LVDS common mode voltage		-	0.7	-	1.6	V
V_{ID}	LVDS swing voltage		-	±100	-	±600	mV
mini-LVDS DC Specifications							
V_{OD}	Output differential voltage range		RL=100Ω (T_A=25℃)	100	-	600	mV
	Output differential voltage deviation			V_{OD_CODE} *0.85(1)	-	V_{OD_CODE} *1.15(1)	mV
V_{OS}	Output offset voltage range			0.6	-	1.3	V
	Output offset voltage deviation			V_{OS_CODE} -0.2(1)	-	V_{OS_CODE} +0.2(1)	V
D_{CLK}	Output clock duty		-	45	50	55	%

Note: (1) The V_{OD_CODE} and V_{OS_CODE} can be programmable by different panel characteristics through ROM code.

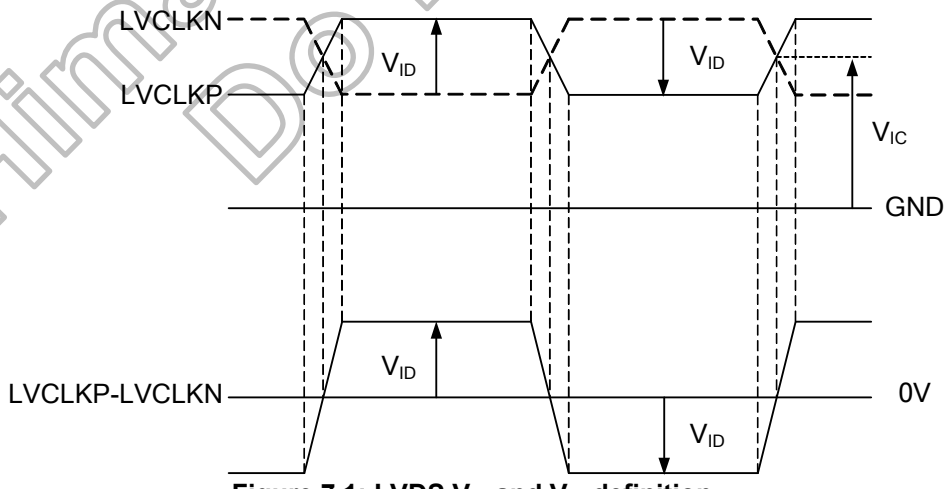


Figure 7.1: LVDS V_{ID} and V_{IC} definition

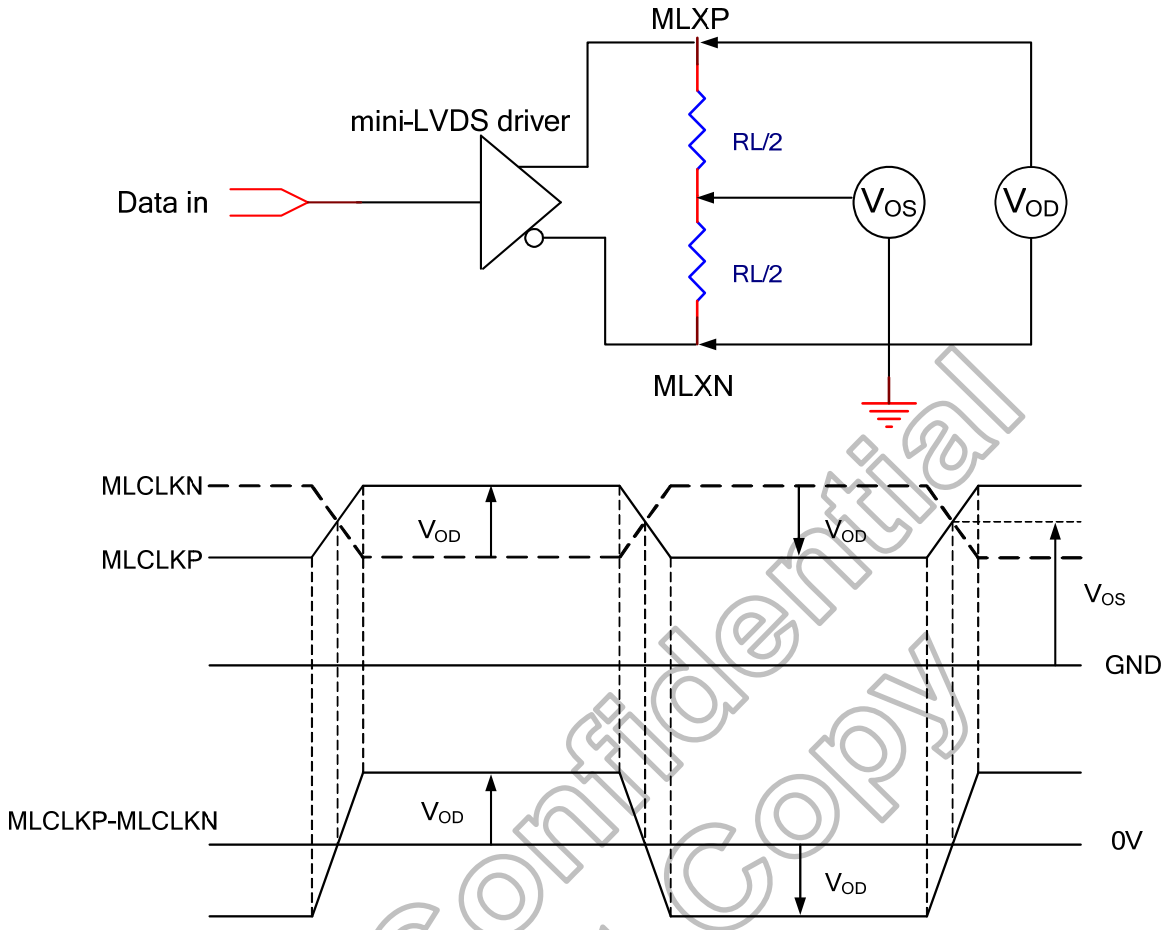


Figure 7.2: mini-LVDS V_{OD} and V_{OS} definition

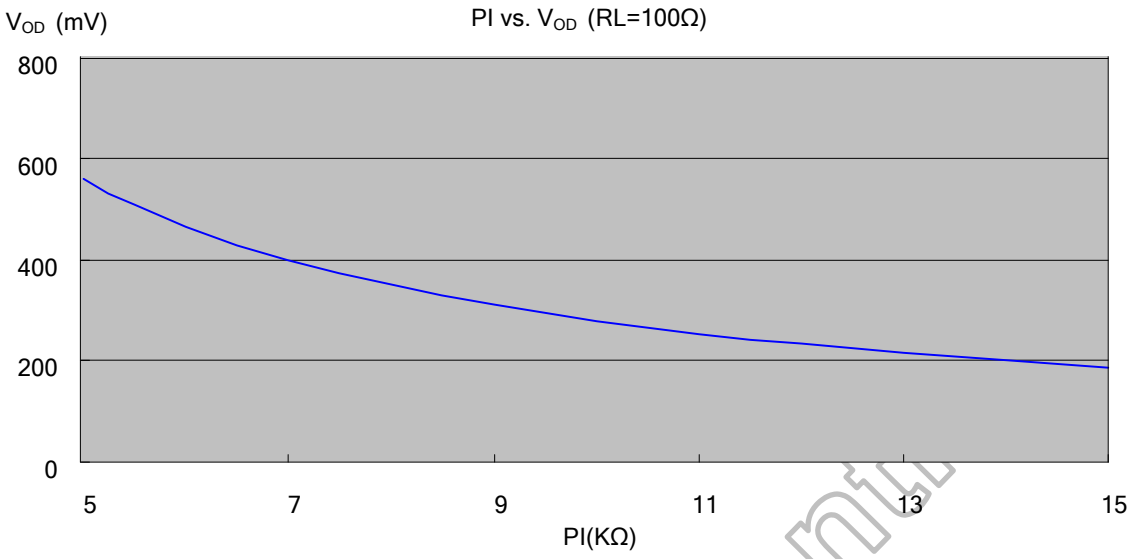


Figure 7.3: PI and V_{OD} relation curve

7.4 ESD parameters

Parameter	Symbol	Spec.	Unit
Human Body Model	HBM	2000	V
Machine Model **(C=200pF, R=0Ω)**	MM	200	V

8. AC Characteristics

8.1 LVDS AC electrical characteristics

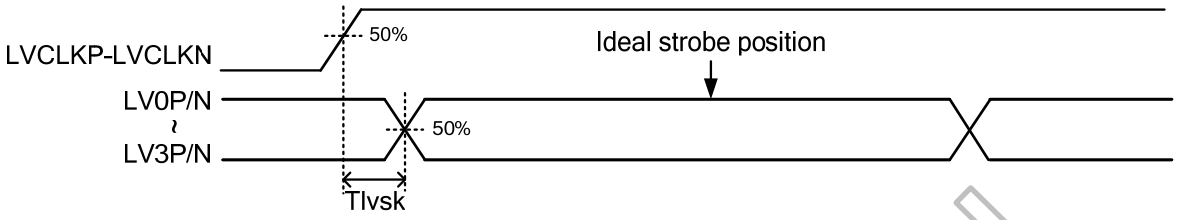


Figure 8.1: LVDS channel to channel skew

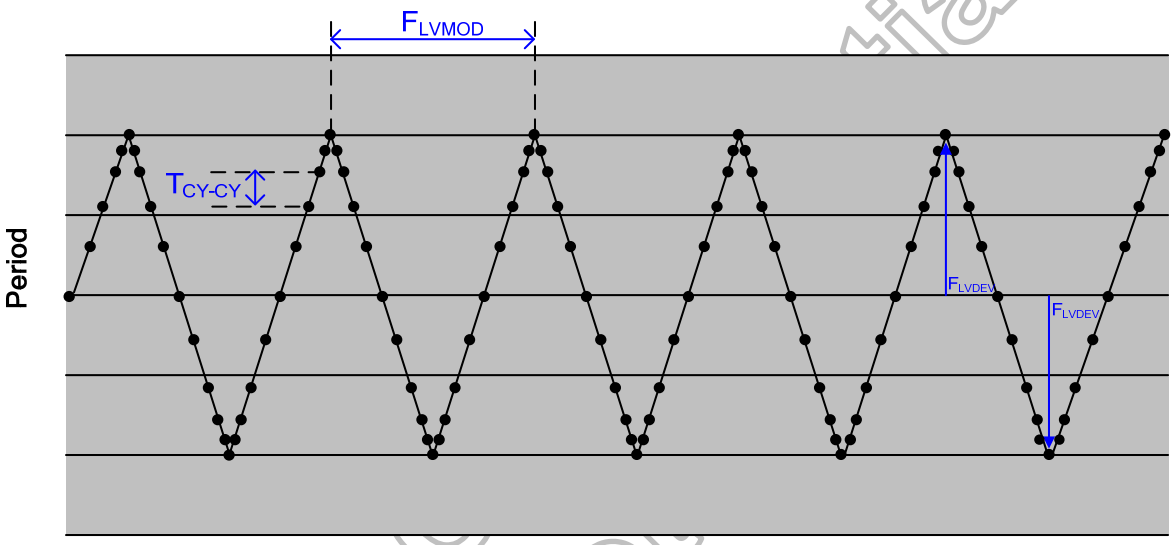


Figure 8.2: LVDS input SSC

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
F	LVDS Input frequency	-	25	-	110	MHz
T_{LVSK}	LVDS channel to channel skew	F=65MHz V_{IC}=1.2V V_{ID}=±200mV	-600	-	+600	ps
F_{LVMOD}	Modulating frequency of input clock during SSC	F=85MHz V_{IC}=1.2V V_{ID}=±200mV	10	-	300	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to cycle jitter		-	-	200	ps

Phase Lock Loop wake-up time

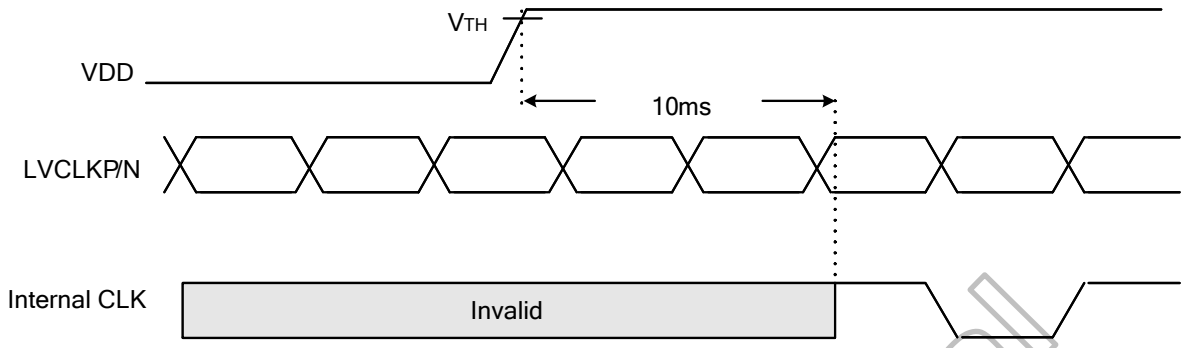


Figure 8.3: PLL wake up time

Power up sequence

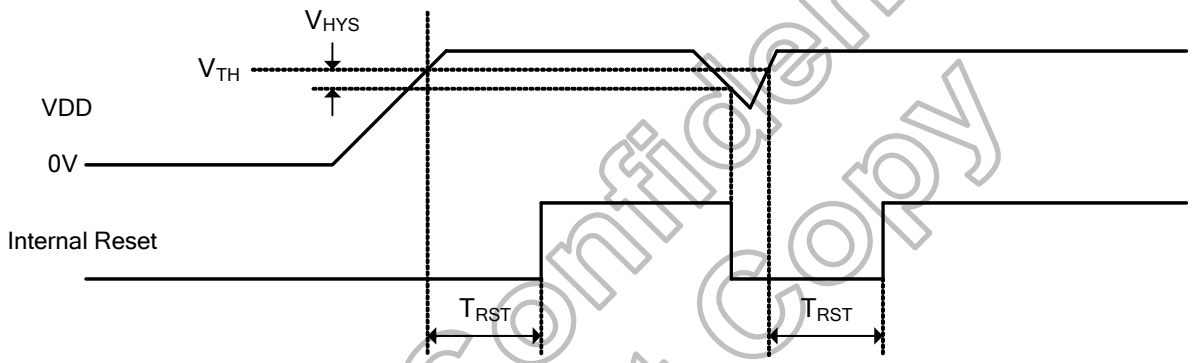
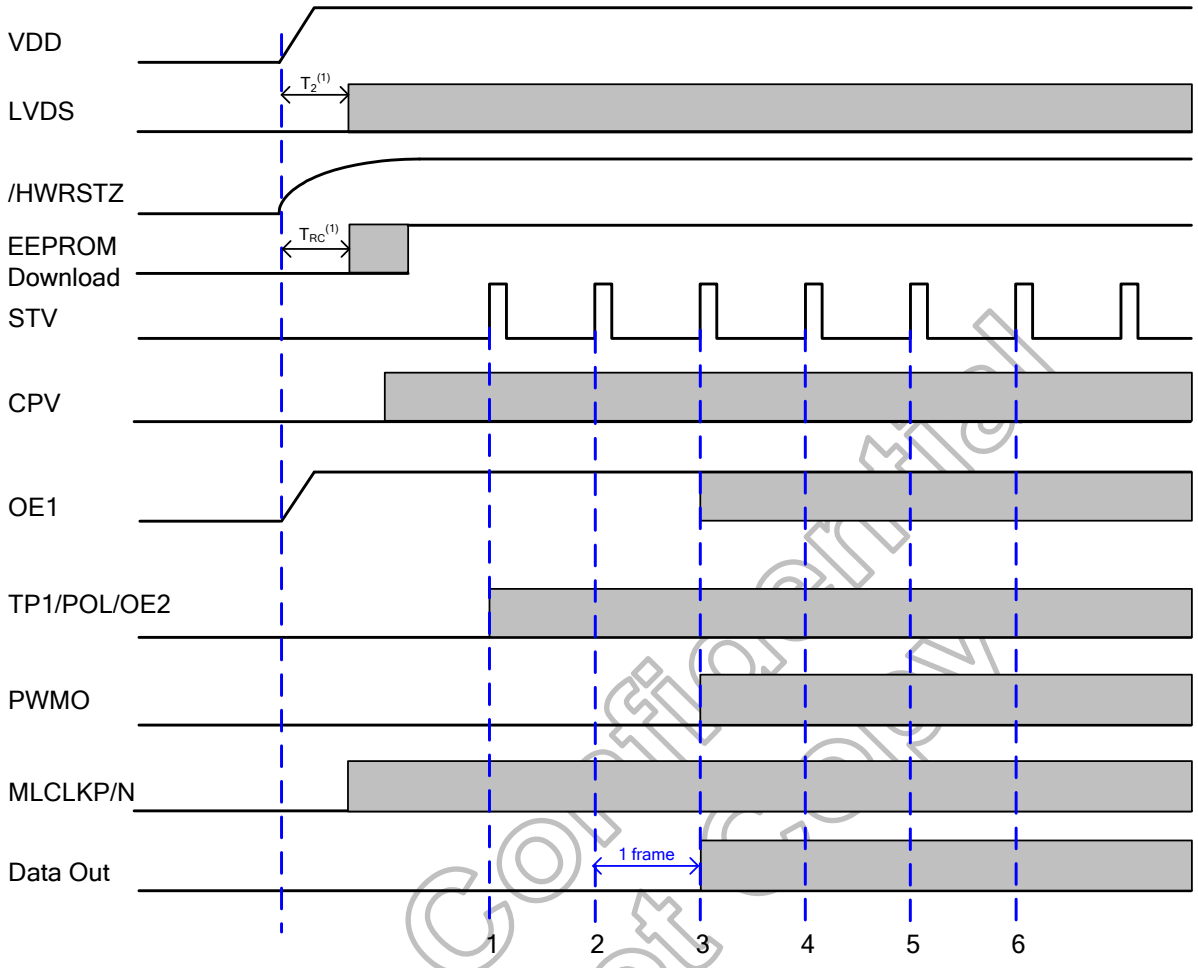


Figure 8.4: Power on reset

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
V_{TH}	Reset threshold voltage	-	1.7	1.9	2.1	V
V_{HYS}	Hysteresis voltage	-	200	-	-	mV
T_{RST}	Time constant of RC	-	-	0.8RC	-	s



Note: (1) 0ms < T_2 < 50ms, T_2 <T_{RC}

Figure 8.5: Power up sequence

8.2 mini-LVDS AC electrical characteristics

8.2.1 mini-LVDS output data format

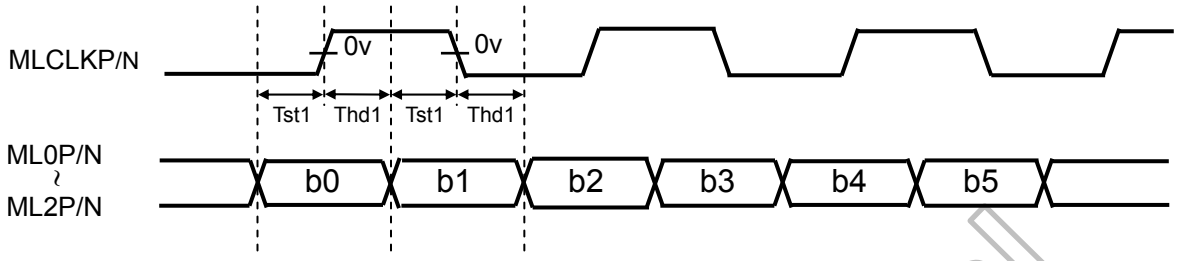


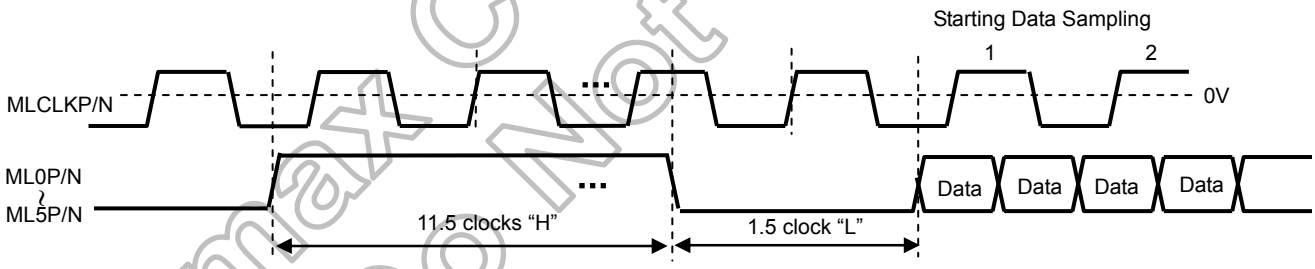
Figure 8.6: mini-LVDS output data format

mini-LVDS skew control

mini-LVDS output skew can be adjusted by ROM code setting

SKEW	Setup time(Tst1)	Hold time(Thd1)	Unit
0	4T/16	4T/16	T (mini-LVDS clock cycle)
1	3T/16	5T/16	
2	2T/16	6T/16	
3	1T/16	7T/16	
4	5T/16	3T/16	
5	6T/16	2T/16	
6	7T/16	1T/16	

mini-LVDS reset pulse



8.2.2 mini-LVDS output data mapping @ WXGA (1366X768)

8.2.2.1 Normal mode

Single port 3-pair

Data pair	One line data										
ML0P/N	1R	2R	3R	4R	5R	6R	7R	8R	---	1365R	1366R
ML1P/N	1G	2G	3G	4G	5G	6G	7G	8G	---	1365G	1366G
ML2P/N	1B	2B	3B	4B	5B	6B	7B	8B	---	1365B	1366B

8.2.2.2 Dual-gate mode

Support four types of dual gate mapping

Pattern A

Dual gate data mapping		ML0	ML1	ML2
Type 0	Odd line	1R	1B	2G
	Even line	1G	2R	2B
Type 1	Odd line	1R	2R	2G
	Even line	1G	1B	2B
Type 2	Odd line	1G	1B	2G
	Even line	1R	2R	2B
Type3	Odd line	1R	2R	2B
	Even line	1G	1B	2G

Pattern B

Dual gate data mapping		ML0	ML1	ML2
Type 0	Odd line	1G	2R	2B
	Even line	1R	1B	2G
Type 1	Odd line	1G	1B	2B
	Even line	1R	2R	2G
Type 2	Odd line	1R	2R	2B
	Even line	1G	1B	2G
Type3	Odd line	1G	1B	2G
	Even line	1R	2R	2B

8.3 mini-LVDS output data swap by ROM code setting

The HX8861-H11 supports 2 swap types for 3-pair mini-LVDS output, including PN and Port swap. All these swapping settings are independent. Users can combine each swapping setting.

8.3.1 3-pair mini-LVDS data swap

Pin no.	Pin name	SWAP V PN Port	SWAP PN V Port
28	ML0P	ML0N	ML2P
27	ML0N	ML0P	ML2N
30	ML1P	ML1N	ML1P
29	ML1N	ML1P	ML1N
32	ML2P	ML2N	ML0P
31	ML2N	ML2P	ML0N
26	MLCLKP	MLCLKN	MLCLKP
25	MLCLKN	MLCLKP	MLCLKN

8.4 SSCG AC electrical characteristics

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
F_{MOD}	Modulation frequency	LVDS input frequency=80MHz	-	125	-	KHz
F_{DEV}	Spread range	LVDS input frequency=80MHz ROM code Setting 0	-	1	-	%
		LVDS input frequency=80MHz ROM code Setting 1	-	2	-	
		LVDS input frequency=80MHz ROM code Setting 3	-	3	-	

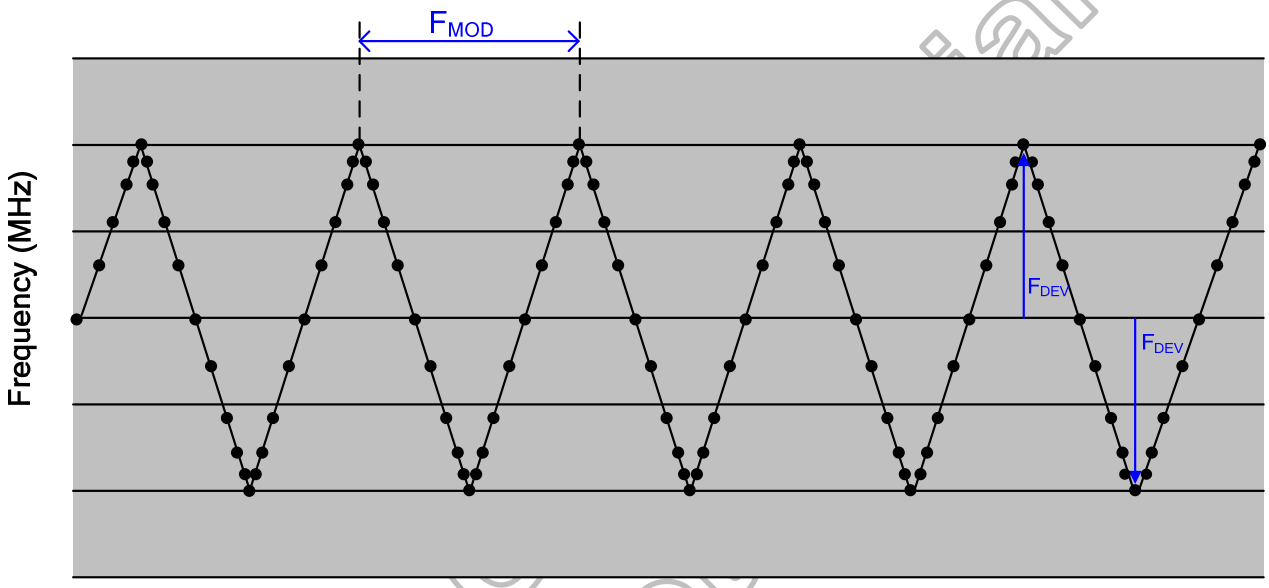
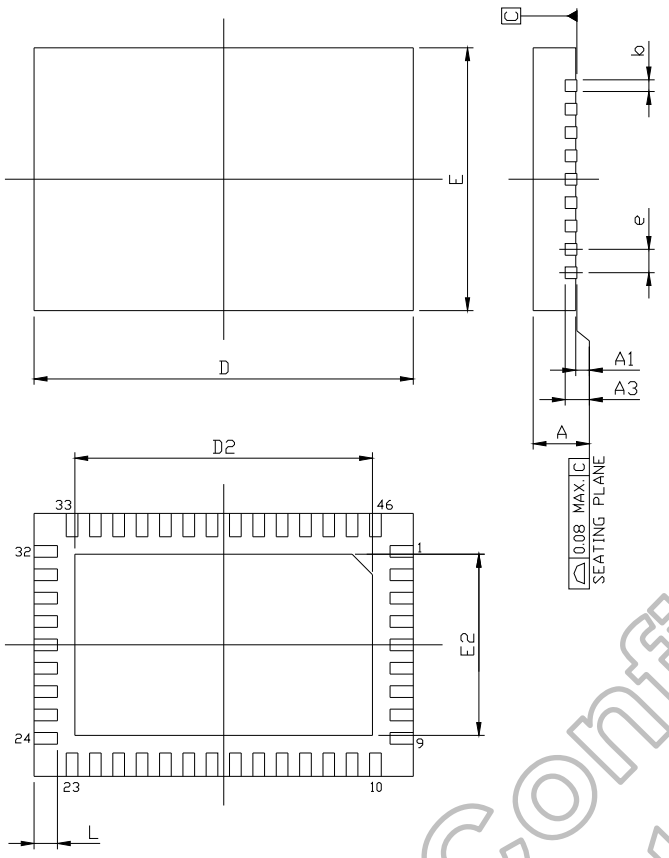


Figure 8.7: SSCG profile

8.5 Oscillator AC electrical characteristics

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
F_{OSC}	Oscillator frequency	-	F_{OSC}*0.85	F_{OSC}	F_{OSC}*1.15	MHz

9. Package Outline Dimension



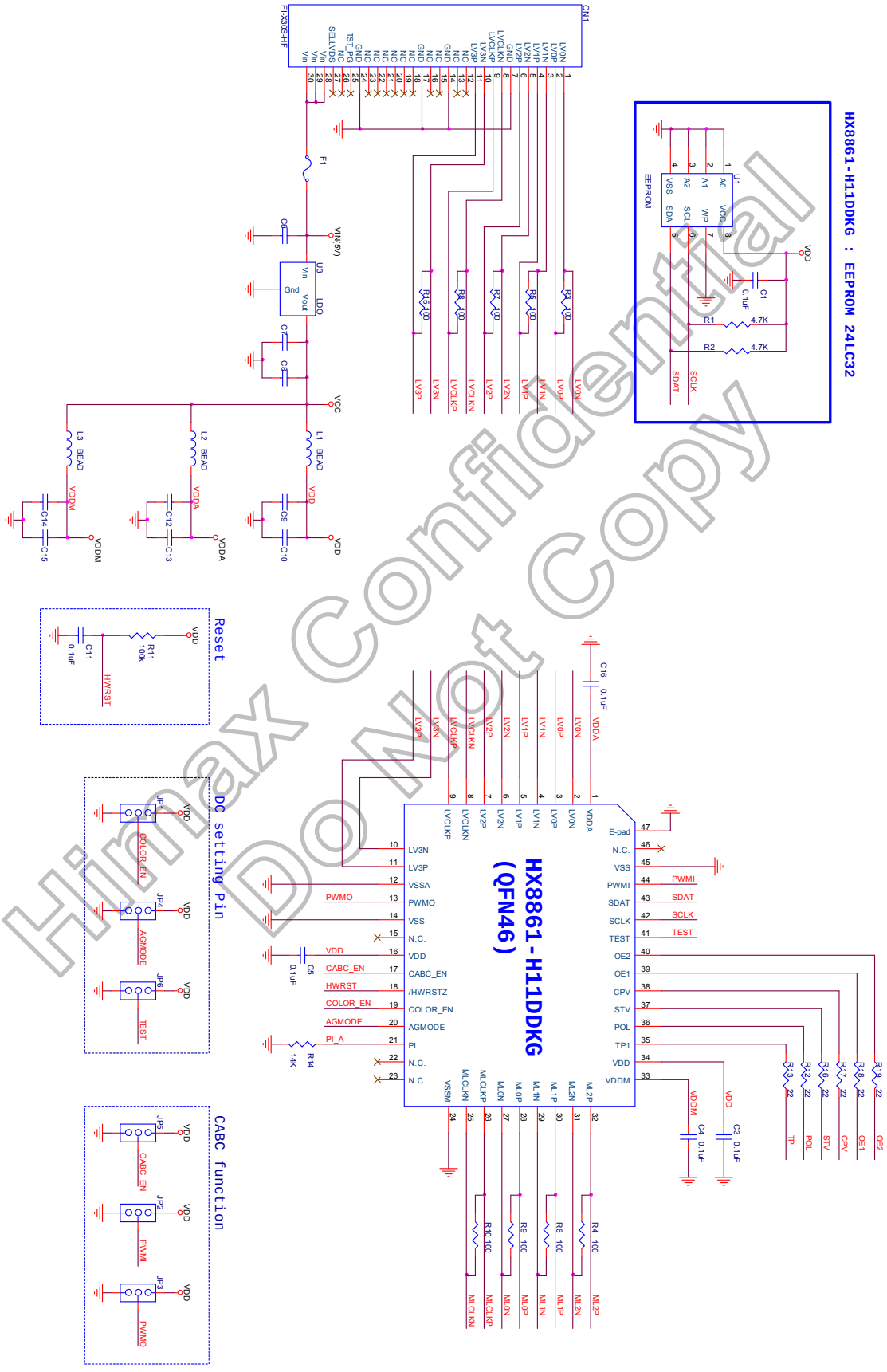
SYMBOLS	MIN.	NOM.	MAX.
A	0.7	–	0.9
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		6.50 BSC	
E		4.50 BSC	
e		0.40 BSC.	
L	0.30	0.40	0.50

Exposed Pad Size					
D2			E2		
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
4.95	5.10	5.25	2.95	3.10	3.25

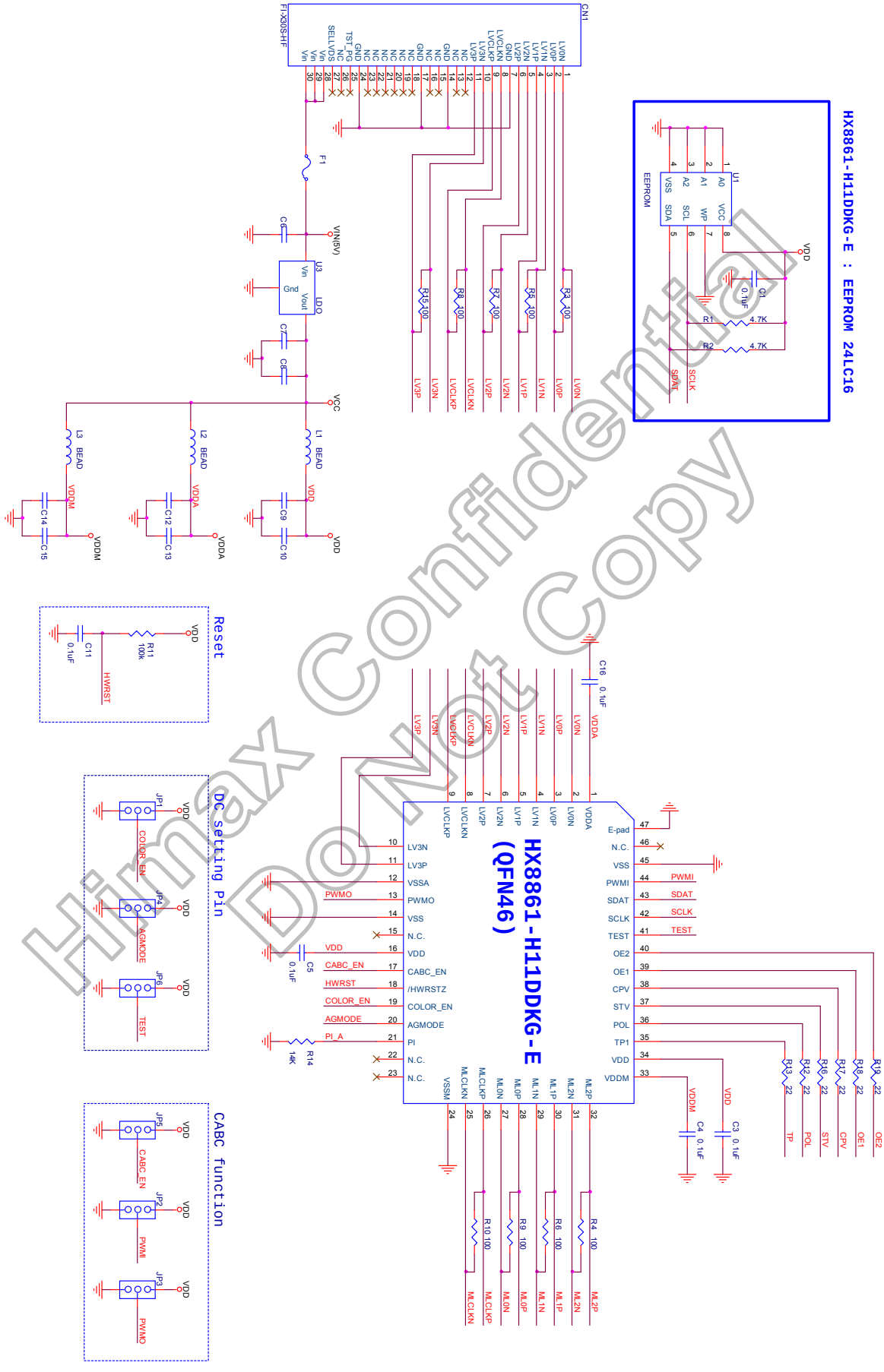
NOTES :
1. JEDEC OUTLINE : MO-220

10. Reference Circuit

10.1 HX8861-H11DDKG



10.2 HX8861-H11DDKG-E



11. Ordering Information

Device	Package	Description
HX8861-H11DDKG	46-pin QFN green package	Support ≧32K bit EEPROM only
HX8861-H11DDKG-E	46-pin QFN green package	Support 2K to 16K bit EEPROM only

12. Revision History

Version	Date	Description of Changes
01	2012/01/16	New setup.
02	2012/06/19	Page 2, 24, 25 Add HX8861-H11DDKG-E: support 2K to 16K bit EEPROM only.
03	2014/05/27	All pages Remove ‘preliminary’ wording. Page 14 Fill spec. in “Supply current (I_{DD})“ Modify “mini-LVDS DC specifications”. Page 23 Modify spec. of “Oscillator frequency(F_{OSC})”